P.S.R. ENGINEERING COLLEGE

(An Autonomous Institution & Affiliated to Anna University, Chennai)

SIVAKASI - 626140

M.E. APPLIED ELECTRONICS

PG REGULATION-2012

CURRICULUM AND SYLLABI

[1st To 4th Semester]

THIS IS THE FINAL VERSION OF THE SYLLABUS AS APPROVED BY THE ACADEMIC COUNCIL OF THE COLLEGE IN THE MEETING HELD ON 1ST JUNE 2013

REGULATIONS FOR PG PROGRAMME (M.E/M.C.A/M.B.A) CANDIDATES ADMITTED DURING THE
ACADEMIC YEAR 2012 - 2013 AND ONWARDS

PRELIMINARY DEFINITIONS AND NOMENCLATURE

In these Regulations, unless the context otherwise requires:

i. "**Programme**" means Post graduate Degree Programme (M.E., M.C.A. and M.B.A)

ii. **"Branch**" means specialization or discipline of M.E. Degree Programme like "Applied Electronics", "Computer Science and Engineering", etc.

iii. "**Course**" means Theory or Practical subject that is normally studied in a semester, like Applied Mathematics, Embedded System Design, etc.

iv. "**Head of the Institution**" means the Principal of a College / Institution who is responsible for all academic activities of that College / Institution and for implementation of relevant Rules and Regulations.

v. **"Head of the Department"** means Head of the Department concerned.

vi. "**Controller of Examinations"** means the Authority of the College who is responsible for all activities of the Examinations.

vii. "**University**" means ANNA UNIVERSITY.

viii. **"College"** or **"Institution"** means P.S.R. Engineering College.

1. ADMISSION REQUIREMENTS

1.1 Candidates for admission to the first semester of the Master's Degree Programme shall be required to have passed an appropriate Degree Examination of Anna University or any other examination of any University or authority accepted as equivalent thereto.

1.2 Eligibility conditions for admission such as class obtained, number of attempts in qualifying examination and physical fitness will be as prescribed from time to time.

1.3 and any other conditions as notified by the Government of Tamil Nadu.

2. PROGRAMMES OFFERED AND MODE OF STUDY

2.1. P.G. PROGRAMMES OFFERED

- M.E. Computer Science and Engineering
- M.E. Structural Engineering
- M.E. Applied Electronics
- M.C.A
- M.B.A

2.2. MODE OF STUDY

Full Time only.

Candidates admitted should be available in the College/ Institution/ University during the complete working hours for curricular, co-curricular and extra-curricular activities assigned to them.

3. DURATION AND STRUCTURE OF THE P.G.PROGRAMMES

3.1 The minimum and maximum periods for completion of the PG Programmes are given below:

Programme	Min. No. of Semesters	Max. No. of Semesters
M.E (Full Time)	4	8
M.B.A	4	8
M.C.A	6	12

The Curriculum and Syllabi of all the P.G. Programmes shall be approved by the Academic Council of the College. The number of Credits to be earned for the successful completion of the programme shall be as specified in the Curriculum of the respective specialization of the P.G. Programme.

3.2 Credits will be assigned to the courses for different modes of study as given below:

3.2.1 The following will apply to all modes of P.G. Programmes.

- One credit for each lecture period allotted per week
- One credit for each tutorial period allotted per week
- One credit for each seminar/practical session of two periods designed per week.

3.2.2 The minimum prescribed credits required for the award of the degree shall be within the limits specified below:

PROGRAMME	PRESCRIBED CREDIT RANGE
M.E. (Full Time)	65 to 75
M.C.A	118
M.B.A	90

3.3 The P.G. Programmes will consist of:

- core subjects
- elective subjects
- project work / thesis / Dissertation
- The Programme will also include design projects / planning projects / seminars / practicals / practical training, if they are specified in the Curriculum.

3.4 The Curriculum and Syllabi of all the P.G. Programmes shall be approved by the Academic Council of the College.

3.5 A student shall pass all the subjects specified in the curriculum of the programme for the successful completion of the programme.

3.6. Each semester shall normally consist of 90 working days or 450 hours or 540 periods of 50 minutes duration. The Head of the Institution shall ensure that every teacher imparts instruction as per the number of periods specified in the syllabus and that the teacher teaches the full content of the specified syllabus for the course (subject) being taught. End-Semester Examination will ordinarily follow immediately after the last working day of the semester.

3.7 The maximum marks assigned to different courses shall be as given below:

3.7.1. i. Each of the theory subjects (excluding project work) shall carry maximum of 100 marks out of which the internal assessment will carry 25 marks, while the end semester Examination will carry 75 marks. The practical classes for all the Practical/Lab component subjects will be assessed continuously and marks will be entered in the prescribed proforma. The progress of Practical classes will be monitored by a committee formed by the concerned Head of the Departments / Professor in-charge of the course to ensure that the concerned staff conducts the laboratory experiments as specified in the syllabus. The maximum marks for the Practical/Lab component courses shall be 100, out of which the continuous internal assessment will carry 25 marks, while the end semester practical examination will carry 75 marks. The award of the end semester practical examination marks shall be conducted by both the Internal and External examiners.

ii. The project report / Thesis / Dissertation of M.E. programme, during Phase I, will be evaluated based on the report and a viva-voce examination by an Internal Examiner and an External Examiner.

iii. The project work / Thesis / Dissertation of M.E. programme, during Phase II, will be evaluated based on the Project Report and a viva-voce examination by a team consisting of the supervisor / Internal Examiner and External Examiner for each specialization.

The project report / Thesis / Dissertation of M.B.A. programme (no phases), will be evaluated based on the report and a viva-voce examination by an Internal Examiner and an External Examiner.

iv. Practical Training / Summer Project if specified in the Curriculum shall not exceed the maximum duration of 4 weeks and should be organized by the Head of the Department for every student.

Practical Training / Summer Project of M.B.A. programme if specified in the Curriculum shall not exceed the maximum duration of 6 weeks and should be organized by the Head of the Department for every student.

v. At the end of Practical Training / Summer Project the candidate shall submit a certificate from the organization where he/she has undergone training and also a brief report. The evaluation will be made based on this report and a Viva-Voce Examination, conducted internally by a Departmental Committee constituted by the Head of the Institution. Certificates submitted by the students shall be attached to the mark list sent by the Head of the Institution.

3.7.2 The electives from the curriculum are to be chosen with the approval of the Head of the Department.

3.7.3 A candidate may be permitted by the Head of the Department to choose one or two subjects from P.G. Programmes offered from other departments in the college / institution during the period of his / her study, provided the Head of the Department offering such course also agrees and there is no clash in the time-table for the lecture classes.

3.8. PROJECT WORK/THESIS *I* DISSERTATION

3 .8.1 Project work / Thesis / Dissertation shall be carried out under the supervision of a qualified teacher in the Department concerned.

3.8.2 A candidate may, however, in certain cases, be permitted to work on the project in an Industrial/Research Organization, on the recommendations of Head of the Department, with the approval of the Head of the Institution. In such cases, the Project work shall be jointly supervised by a supervisor of the department and an Engineer / Scientist from the Organization and the student shall be instructed to meet the supervisor periodically and to attend the review committee meetings for evaluating the progress.

3.8.3 The Project work / Thesis / Dissertation (Phase-II) shall be used for a minimum of 16 weeks during the final semester from the next day of viva voce examination of Phase-1 Project.

The Project work / Thesis / Dissertation of M.B.A programme shall be used for a minimum of 16 weeks during the final semester.

3.8.4 The Project Report / Thesis / Dissertation report / Drawings prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted at the end of the IV semester. The last date for the submission of Thesis (Phase-II) will be six months from the last date of the submission of Phase-I Project Report or Third Semester examination or 24 months from the date of commencement of First Semester class work, whichever is later. However, in exceptional cases, based on the recommendation of the Professor-in-charge of the course the Chairman, Academic Council can permit an extension of time not exceeding 31 days. If a candidate submits the project report/ thesis report/ dissertation after the specified deadline, he ***I*** she is deemed to have failed in the Project Work / Thesis ***I*** Dissertation and shall re-enroll for the same in a subsequent semester.

For M.B.A programme, the Project Report / Thesis / Dissertation report / Drawings prepared according to approved guidelines and duly signed by the supervisor(s) and the Head of the Department shall be submitted at the end of the IV semester. The last date for the submission of Thesis will be six months from the commencement of fourth semester. However, in exceptional cases, based on the recommendation of the Professor-in-charge of the course the Chairman, Academic Council can permit an extension of time not exceeding 31 days. If a candidate submits the project report ***I*** thesis report/ dissertation after the specified deadline, he ***I*** she is deemed to have failed in the Project Work / Thesis ***I*** Dissertation and shall re-enroll for the same in a subsequent semester.

3.8.5 Every candidate doing M.E. shall, based on his ***I*** her project work thesis disserta tion, send a paper for publication in a journal or a conference in which full papers are published after usual review. An acknowledgement for having communicated to the journal or conference shall be attached to the report of the project work ***I*** thesis ***I*** dissertation. Such acknowledgements shall be sent to the Office of the Controller of Examinations along with the evaluation marks by the team of examiners without which the marks shall not be accepted.

3.8.6 A student who has passed in all the courses prescribed in the curriculum for the award of the degree shall not be permitted to re-enroll to improve his/her marks in a course or the aggregate marks.

3.8.7 The medium of instruction, examination, seminar and project ***I*** thesis ***I*** dissertation reports shall be English.

4. FACULTY ADVISER

To help the students in planning their courses of study and for general advice on the academic programme, the Head of the Department will attach a certain number of students to a teacher of the Department who shall function as Faculty Adviser for those students throughout their period of study. Such Faculty Adviser shall advise the students and monitor the subjects taken by the students, check the attendance and progress of the students attached to him *I* her and counsel them periodically. If necessary, the faculty adviser may also discuss with or inform the parents about the progress of the students.

5. CLASS COMMITTEE

5.1 A Class Committee consists of teachers of the concerned class, student representatives and a chairperson who is not teaching the class. It is like the 'Quality Circle' (more commonly used in industries) with the overall goal of improving the teaching-learning process. The functions of the class committee include Solving problems experienced by students in the class room and in the laboratories.

- Clarifying the regulations of the degree programme and the details of rules therein.
- Informing the student representatives the academic schedule including the dates of assessments and the syllabus coverage for each assessment.
- Informing the student representatives the details of regulations regarding the weightage used for each assessment. In the case of practical courses (Iaboratory/ drawing/ project work/ seminar etc.) the breakup of marks for each experiment/ exercise/ module of work, should be clearly discussed in the class committee meeting and informed to the students.
- Analyzing the performance of the students of the class after each test and finding the ways and means of solving problems, if any.
- Identifying the weak students, if any, and requesting the teachers concerned to provide additional help or guidance or coaching to such weak students.

5.2 The class committee for a class under a particular specialization is normally constituted by the Head of the Department. However, if the students of different specializations are mixed in a class, the class committee is to be constituted by the Head of the Institution.

5.3 The class committee shall be constituted on the first working day of any semester or earlier.

5.4 At least 2 student representatives (usually 1 boy and 1 girl) shall be included in the class committee.

5.5 The chairperson of the class committee may invite the Faculty Adviser(s) and the Head of the Department to the meeting of the class committee.

5.6 The Head of the Institution may participate in any class committee of the institution.

5.7 The chairperson is required to prepare the minutes of every meeting, submit the same to the Head of the Institution within two days of the meeting and arrange to circulate among the concerned students and teachers. If there are some points in the minutes requiring action by the management, the same shall be brought to the notice of the management by the Head of the Institution.

5.8 The first meeting of the class committee shall be held within one week from the date of commencement of the semester, in order to inform the students about the nature and weight age of assessments within the framework of the Regulations. Two or three subsequent meetings may be held at suitable intervals. During these meetings the student members representing the entire class, shall meaningfully interact and express the opinions and suggestions of the class students to improve the effectiveness of the teaching-learning process.

6. COURSE COMMITTEE FOR COMMON COURSES

Each common theory course offered to more than one group of students shall have a "Course Committee" comprising all the teachers teaching the common course with one of them nominated as Course Coordinator. The nomination of the Course Coordinator shall be made by the Head of the Department /Head the Institution depending upon whether all the teachers teaching the common course belong to a single department or to several departments. The "Course committee" shall meet as often as possible and ensure uniform evaluation of the tests and arrive at a common scheme of evaluation for the tests. Wherever it is feasible, the course committee may also prepare a common question paper for the test(s).

7. PROCEDURES FOR AWARDING MARKS FOR INTERNAL ASSESSMENT

7.1 Every teacher is required to maintain an 'ATTENDANCE AND ASSESSMENT RECORD' which consists of attendance marked in each lecture or practical or project work class, the test marks and the record of class work (topic covered), separately for each course. This should be submitted to the Head of the Department periodically (at least three times in a semester) for checking the syllabus coverage and the records of test marks and attendance. The Head of the Department will put his signature and date after due verification. At the end of the semester, the record should be verified by the Head of the Institution who will keep this document in safe custody (for five years).

7.2 Theory Subjects [25 marks)

(a). Unit Tests [60% weightage]:

Three tests each carrying sixty (60) marks shall be conducted by the Department / Institution. The total marks obtained in all the tests put together out of 180, shall be reduced to 60 marks and rounded to nearest integer (this implies equal weightage to all the three tests). However a retest at the discretion of the Head of the Department may be conducted for the deserving candidates.

(b). Assignment/Seminar/Miniproject [30% weightage]:

A student has an option to choose any one of the following:

i) Assignment:

Two assignments each carrying 15 marks and requiring work of average 5 to 6 hours of study and written work of average 5 to 6 hours shall be given to be carried out by each student in a separate assignment folder, duly indexed with headings, date of submission, marks, remarks and signature of faculty with date etc.

ii) Assignment and Seminar:

A student has to carry out one assignment and one seminar each carrying 15 marks each. An assignment normally requires work of average 5 to 6 hours of study and written work of average 5 to 6 hours which has to be submitted in a separate assignment folder, duly indexed with headings, date of submission, marks, remarks and signature of faculty with date etc. The student has to make one technical seminar on current topics related to the specialization. The students are expected to submit a report his/her presentation. The seminar will be assessed by the course tutor

with common parameters as described by the department.

iii) Mini project

A student can carry out mini project carrying 30 marks either in hardware or software with the approval of the head of the department. The student has to submit a report before the end of the semester. Mini project will be assessed based on the model, presentation and report as decided by the department.

(c). Attendance [10% weightage]:

A maximum of 10 marks for attendance out of 100 marks shall be given to each student depending on his / her attendance percentage as per the distribution given below:

Percentage of Attendance	Marks
75	2
76 – 80	4
81 – 84	6
85 – 90	8
91 and above	10

7.3 Practical Subjects [25 marks)

Every practical exercise / experiment shall be evaluated based on conduct of exercise / experiment and records maintained. There shall be at least one test.

The criteria for determining the internal assessment marks are:

Experiment / Record / Average Practical classes' performance: 50 % Weightage
Practical Test : 40 % Weightage
Attendance : 10 % Weightage

Total 100 marks shall be reduced to 25 Marks.

7.4 Theory Subjects with Laboratory Component

(a). Unit Tests [60% weightage]:

If there is a theory subject with Laboratory component, there shall be three tests; the first two tests (each 60 Marks) will be from theory portions and third test (maximum mark 60) will be for laboratory component. The total 180 marks should be reduced to 60 marks. However a retest at the discretion of the Head of the Department may be conducted for the deserving candidates.

(b). Assignment [30% weightage]:

Two assignments each carrying 15 marks and requiring work of average 5 to 6 hours of study and written work of average 5 to 6 hours shall be given to be carried out by each student in a separate assignment folder, duly indexed with headings, date of submission, marks, remarks and signature of faculty with date etc.

(c). Attendance [10% weightage]:

A maximum of 10 marks for attendance out of 100 marks shall be given to each student depending on his / her attendance 'percentage as per the distribution given below:

Percentage of Attendance	Marks
75	2
76 – 80	4
81 – 84	6
85 – 90	8
91 and above	10

7.5 M.E. Project Work

There shall be a minimum of two reviews for both Phase-I and Phase-II to be conducted separately. The internal and external marks distribution for each phase is given in the table below. The student shall make presentation on the progress made before the review committee. The Head of the Institution/Department shall constitute a review committee for each branch of study.

Project (M.E)	Internal (25 %)		External (75%)	
	Review-I	Review-II	Thesis by External	Viva-voce
Phase-I	25	25	60	90
Phase-II	50	50	120	180

M.B. A/M.C.A. Project Work

There shall be a minimum of two reviews and a model viva-voce for Project Work to be conducted with internal 100 marks and external 300 marks. The student shall make presentation on the progress made before the review committee. The Head of the Institution / Department shall constitute a review committee.

Project work (M.B.A/M.C.A)	Internal (25 %)			External (75%)	
	Review-I	Review-II	Viva-voce	Project Report	Viva-voce
	25	25	50	120	180

8. REQUIREMENTS FOR COMPLETION OF A SEMESTER

A candidate who has fulfilled the following conditions shall be deemed to have satisfied the requirements for completion of a semester.

8.1 A candidate will be permitted to appear for the Examination for any semester, only if

i) he / she secures not less than 75% of attendance in the number of working days during that semester, provided that it shall be open to Chairman of the Academic Council and any authority delegated with such powers (by the governing body) to grant exemption (based on the recommendation of the Head of the Department) to a candidate who has

failed to secure 75% of the attendance for valid reasons and has secured not less than 65% of the attendance. Such exemptions can be allowed only ONCE during his/ her entire course of study.

ii) Candidates representing University in State / National/International/Inter University Sports events, Co & Extra - Curricular activities, paper or project presentation with prior permission from the Head of Institution are given exemption up to 10% of the required attendance and such candidates shall be permitted to appear for the current semester examination.

iii) his / her conduct has been certified to be satisfactory by the concerned Head of Department.

iv) Condonation can be allowed only ONCE during his/ her entire course of study.

8.2 Candidates who do not complete the semester (as per clause 8.1), will not be permitted to write the end-semester examination and are not permitted to go to next semester. They are required to repeat the incomplete semester in a subsequent academic year after getting the necessary permission from the authorities.

9. REQUIREMENTS FOR APPEARING FOR SEMESTER EXAMINATION

A candidate shall normally be permitted to appear for the semester examination of the current semester if he/she has satisfied the semester completion requirements (Subject to Clause 8.1) and has registered for examination in all courses of that semester. Registration is mandatory for all arrear subjects along with current semester subjects, failing which the candidate will not be permitted to move to the higher semester.

10. END SEMESTER EXAMINATION

10.1 There shall be one end-semester examination of 3 hours duration for each lecture based course.

10.2 The project report / Thesis / Dissertation of M.E. programme, during Phase I, will be evaluated based on the report and a viva-voce examination by an Internal Examiner and an External Examiner.

10.3 The project work / Thesis *I* Dissertation of M.E. programme, during Phase II, will be evaluated based on the Project Report and a viva-voce examination by a team consisting of the supervisor / Internal Examiner and an External Examiner for each specialization.

The following will be the weightages for different courses.

Lecture or Lecture cum Tutorial	
Internal Assessments	25%
Semester Examination	75%
Laboratory based subjects	
Internal Assessments	25%
Semester Examination	75%
Project work	
Internal Assessment	25%
Evaluation of Project Report by external examiner	30%
Viva- Voce Examination (by both Internal & External Examiners)	45%

M.E.Project

(i). For PHASE- I [Maximum Marks: 200]

Internal Assessment:	50 Marks [Guide: 50 %, Committee: 50%]]
Semester Examination:	150 Marks [Evaluation: 60 Marks, Viva-Voce: 90Marks]

(ii). For Phase- II [Maximum Marks: 400]

Internal Assessment:	100 Marks [Guide: 50%, Committee: 50%)
Semester Examination:	300 Marks [Evaluation: 120 Marks, Viva-Voce: 180 Marks)

MBA Project [MaximumMarks:400]

Internal Assessment:	100 Marks
Semester Examination:	300 Marks [Evaluation: 120 Marks, Viva-Voce: 180 Marks)

11. PASSING REQUIREMENTS

11.1. For each subject the examination will be conducted for 100 marks. A candidate who secures not less than 50% *at* the total marks in the End Semester examination and Internal Assessment put together in both theory and Practical subjects, including Project work, subject to securing a minimum of 50% in the End - Semester examination, wherever applicable, shall be declared to have passed the examination in that subject. When the mark secured *tor* 100 is converted to 75, for a pass minimum 37 marks must be secured.

11.2 If a candidates fails to secure a pass in a particular course it is mandatory that he/she shall register and reappear for the examination in that course during the next semester when examination is conducted in that course; he/she should continue to register and reappear for the examination till he / she secures a pass.

12. MALPRACTICE

If a student indulges in malpractice in any of the end semester examinations, he / she shall be liable for punitive action as and when prescribed by the Anna University.

13. ELIGIBILITY FOR THE AWARD OF THE MASTER'S DEGREE

13.1 A student shall be declared eligible *for* the award *of* the degree if he/she has successfully passed all the subjects as specified by the curriculum corresponding to his / her programme within the stipulated time.

No disciplinary action is pending against him/her.

13.2 The award *of* the degree must have been approved by the University.

14. ISSUE OF MARK SHEETS

Individual mark sheet / grade sheet for each semester will be issued, containing the following information through the Head of the Department concerned, after the publication of the results.

i) The grades obtained in each course.

ii) Whether the candidate has passed / failed in the courses concerned.

15. CLASSIFICATION OF THE DEGREE AWARDED

15.1 A candidate who qualifies for the Degree (vide clause 13) by passing the examination in all subjects of the entire course in first attempt within the specified minimum number of semesters securing an aggregate of not less than 75% (CGPA of not less than 8.5) of the total marks (Internal Assessment plus Semester Examination Marks) shall be declared to have passed the examination for the degree in FIRST CLASS WITH DISTINCTION. For this purpose the withdrawal from examination (vide clause 16) will not be construed as an appearance. Further, the authorized break of study (vide clause 17(iii)) will not be counted for the purpose of classification.

15.2 A candidate who qualifies for the award of the Degree (vide clause 13) having passed the examinations in all the subjects of the course within the specified minimum number of semesters reckoned from his/her commencement of study plus one year securing an aggregate of not less than 60% (CGPA of not less than 6.50) of the total marks (Internal Assessment plus Semester Examination Marks) shall be declared to have passed the examination for the degree in FIRST CLASS. For this purpose, the authorized break of study (vide clause 17(iii)} will not be counted for the purpose of classification.

15.3 All other candidates (not covered in clauses 15.1 and 15.2) who qualify for the award of the degree (vide Clause 13) shall be declared to have passed the examination in Second Class.

15.4 A candidate who is absent in semester examination in a subject *I* project work after having enrolled for the same shall be considered to have appeared in that examination for the purpose of classification.

16. PROVISION FOR WITHDRAWAL FROM EXAMINATION

A candidate may, for valid reasons (medically unfit *I* unexpected family situations), be granted permission to withdraw from appearing for any subject or subjects of only one semester examination during the entire duration of the degree programme. Also only one application for withdrawal is permitted for that semester examination in which withdrawal is sought. Withdrawal application shall be valid only if the candidate is, otherwise, eligible to write the examination and if it is made prior to the commencement of the last examination in that semester and duly recommended by the Head of Department and approved by the Head of the Institution.

Withdrawal shall not be construed as an appearance for the eligibility of a candidate for the purpose of classification vide clause 15.1 and 15.2.

(i) "Withdrawal application is to be made within TEN days prior to the commencement of the examination".
(ii) "Withdrawal is NOT permitted for arrears examinations of the previous semesters".
(iii) Notwithstanding the requirement of mandatory TEN days notice, applications for withdrawal for special cases under extraordinary conditions will be considered on the merit of the case.

17. AUTHORIZED BREAK OF STUDY FROM A PROGRAMME

i) Break of study shall be granted only once for valid reasons (on medical grounds only) for a maximum of one year during the entire period of study of the degree programme. However, in extraordinary situation the candidate may apply for additional break of study not exceeding another one year by paying prescribed fee for break of study. If a candidate intends to temporarily discontinue the programme In the middle of the semester for valid reasons and rejoin the programme in a later semester, permission may be granted based on the merits of the case provided he *I* she applies to the Head of the Institution with recommendation from the concerned HOD in advance, but not later than the last date for reg-

istering for the end semester examination of the semester in question, through the Head of Department stating the reasons therefore and the probable date of rejoining the programme .

ii) However, if the candidate. has not completed the first semester of the programme, break of study will be considered only on valid medical reasons. The candidate permitted to rejoin the programme after the break shall be governed by the rules and regulations in force at the time of rejoining. Such candidates may have to do additional courses prescribed by the Academic Council, if the regulation is changed.

iii) The authorized break of study will not be counted for the duration specified for passing all the courses for the purpose of classification vide Clause 15.1 and 15.2.

iv) The total period for completion of the programme reckoned from, the commencement of the first semester to which the candidate was admitted shall not exceed the maximum period specified in clause 3 irrespective of the period of break of study in order that he / she may be eligible for the award of the degree (vide clause 13).

v) If any student is detained for want of requisite attendance, progress and good conduct, the period spent in that semester shall not be considered as permitted 'Break of Study' and Clause 17(iii)is not applicable for this case.

18. REVALUATION

Copies of answer script for theory subject(s) can be obtained from the Office of the Controller of Examinations on payment of a prescribed fee specified for this purpose through proper application.

A candidate can apply for revaluation of his *I* her semester examination answer paper in a theory course, within a week from the declaration of results, on payment of a prescribed fee through proper application to the Office of the Controller of Examinations, as per the norms given by the Chairman, Academic Council. Revaluation is not permitted for Practical Courses and Project work.

19. RANK OF A STUDENT

A candidate who qualifies for the Degree by passing the examination in all subjects of the entire course in first attempt within a period of two consecutive academic years from the date of admission to the course can be given his position in the class as rank. The Rank is determined from I Semester to IV Semester examination mark percentages.

20. PROCEDURE FOR USING SCRIBER

If a candidate is physically handicapped (in case of accidents / ill health) at the time of examination, then he / she may be permitted to use a scriber to write the examination. In such case 30 minutes extra time will be permitted. The Scriber should be a non-engineering student / graduate.

21. INDUSTRIAL VISIT

Every student is required to undergo one Industrial visit, starting f*rom* the first semester of the Programme. Every teacher shall take the students at least for one industrial visit in a year.

22. DISCIPLINE

Every student is required to observe disciplined and decorous behavior both inside and outside the college and not to indulge in any activity which will tend to bring down the prestige of the College. In the event an act of indiscipline being reported, the Principal shall constitute a disciplinary committee consisting of three Heads of Departments of which one should be from the faculty of the student, to inquire into acts of discipline. The disciplinary action is subject to review by the University in case the student represents to the University. Any expulsion of the student from the college shall be with prior concurrence from Director of Technical Education / University.

23. CREDIT SYSTEM

The letter grade and the grade point are awarded based on percentage of marks secured by a candidate in individual subjects as detailed below:

Range of Total Marks	Letter Grade	Grade Points (GP)
90 to 100	S	10
80 to 89	A	9
70 to 79	B	8
60 to 69	C	7
55 to 59	D	6
50 to 54	E	5
0 to 49	U	0
Incomplete	I	0
Withdrawal	W	0
Absent	AB	0

"U" - denotes failure in the course.
"I" - denotes incomplete as per clause 8.1 and hence prevention from writing End Semester Examination.
"W" - denotes withdrawal from the subject.
"RA" - Reappearance denotes failure in the course.
"AB" - Absent

After results are declared, Consolidated Mark sheets will be issued to each student which will contain the following details:

The list of subjects enrolled during the semester and the grades scored. The Grade Point Average (GPA) for the semester and the Cumulative Grade Point Average (CGPA) of all courses enrolled from first semester onwards.

GPA is the ratio of the sum of the products of the number of credits of courses registered and the points corresponding to the grades scored in those subjects, taken for all the subjects, to the sum of the number of credits of all the subjects in the semester.

$$GPA = \frac{\text{Sum of } [C \times GP]}{\text{Sum of } C}$$

Where, C - credit of a particular subject &
GP - grade point obtained by the student in the respective subjects.

CGPA will be calculated in a similar manner, considering all the subjects enrolled from first semester. 'U", "I", "W' and “AB” grades will be excluded for calculating GPA and CGPA.

Each subject is normally assigned certain number of credits with 1 credit per lecture period per week, 1 credit per tutorial period per week, 1 credit for 2 periods of laboratory or practical or seminar or project work per week (2 credits for 3 or 4 periods of practical).

However, the performance of a student is evaluated only based on the mark system.

.

24. REVISION OF REGULATIONS AND CURRICULAM

The college may from time to time revise, amend or change the regulations, scheme of examinations and syllabi, if found necessary.

PG REGULATION – 2012

M.E. APPLIED ELECTRONICS
CURRICULUM I TO IV SEMESTERS (FULL TIME)
SEMESTER I

Sl.No	Code	Course Title	L	T	P	C
Theory						
1	12AE11	Applied Mathematics for Electronics Engineers	3	1	0	4
2	12AE12	Statistical Digital Signal Processing	3	1	0	4
3	12AE13	Advanced Digital System Design	3	1	0	4
4	12AE14	Microcontrollers & Interfacing	3	0	0	3
5	12AE15	Analysis and Design of Analog Integrated Circuits	3	0	0	3
6	12AE16	Consumer Electronics	3	0	0	3
Practical						
7	12AE17	Electronic System Design lab I	0	0	3	2
TOTAL			18	3	5	23

SEMESTER II

Sl. No	Code	Course Title	L	T	P	C
Theory						
1	12AE21	Embedded System Design	3	0	0	3
2	12AE22	ASIC Design Techniques	3	0	0	3
3	12AE23	Virtual Instrumentation Systems	3	0	0	3
4	12AE24	Digital Control Engineering	3	1	0	4
5	-	Elective I*	3	0	0	3
6	-	Elective II*	3	0	0	3
Practical						
7	12AE25	Electronic System Design lab II	0	0	4	2
8	12AE26	Technical Seminar-1	0	0	2	1
TOTAL			18	2	6	22

SEMESTER III

Sl. NO	Code	Course Title	L	T	P	C
Theory						
1	-	Elective I*	3	0	0	3
2	-	Elective II*	3	0	0	3
3	-	Elective III*	3	0	0	3
Practical						
4	12AE31	Project Work (Phase I)	0	0	12	6
5	12AE32	Technical Seminar-2	0	0	2	1
TOTAL			9	0	14	16

SEMESTER IV

Sl. No	Code	Course Title	L	T	P	C
Practical						
1	12AE41	Project Work (Phase II)	0	0	24	12
TOTAL			0	0	24	12

*** LIST OF ELECTIVES FOR M.E APPLIED ELECTRONICS**

Sl. No	Code	Course Title	L	T	P	C
SEMESTER II						
1.	12AE2A	Computer Architecture and Parallel Processing	3	0	0	3
2.	12AE2B	Digital Image Processing	3	0	0	3
3.	12AE2C	Electro Magnetic Interference & Compatibility in System Design	3	0	0	3
4.	12AE2D	Multimedia Compression and Coding Techniques	3	0	0	3
5.	12AE2E	Opto Electronics	3	0	0	3
6.	12AE2F	Low power VLSI Design	3	0	0	3
7.	12AE2G	Real Time Operating Systems	3	0	0	3
8.	12AE2H	Wireless and Mobile Communication	3	0	0	3
SEMESTER III						
9.	12AE3A	Advanced Robotics & Automation	3	0	0	3
10.	12AE3B	Applied Cryptography and Data Security	3	0	0	3
11.	12AE3C	Bluetooth Technologies	3	0	0	3
12.	12AE3D	Embedded Communication Software Design	3	0	0	3
13.	12AE3E	Embedded Control Systems	3	0	0	3
14.	12AE3F	High Definition Television	3	0	0	3
15.	12AE3G	High Performance Communication Networks	3	0	0	3
16.	12AE3H	Internet Technologies & Application	3	0	0	3
17.	12AE3I	Micro Electro Mechanical System	3	0	0	3
18.	12AE3J	Nano Electronics	3	0	0	3
19.	12AE3K	PC Based Instrumentation control	3	0	0	3
20.	12AE3L	RF System Design	3	0	0	3
21.	12AE3M	RFID and its Applications	3	0	0	3

TOTAL NO. OF CREDITS TO BE EARNED FOR THE AWARD OF DEGREE 23+22+16+12=73

12AE11 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

L T P C
3 1 0 4

UNIT I LINEAR ALGEBRAIC EQUATION AND EIGEN VALUE PROBLEMS 10

System of equations- Solution by Gauss Elimination, Gauss-Jordan and LU decomposition method - Jacobi, Gauss-Seidal iteration method- Eigen values of a matrix by Jacobi and Power method.

UNIT II WAVE EQUATION 10

Solution of initial and boundary value problems- Characteristics- D'Alembert's Solution – Significance of characteristic curves - Laplace transform solutions for displacement in a long string - a long string under its weight - a bar with prescribed force on one end- free vibrations of a string.

UNIT III SPECIAL FUNCTIONS 10

Bessel's equation - Bessel Functions- Legendre's equation - Legendre polynomials -Rodrigue's formula - Recurrence relations- generating functions and orthogonal property for Bessel functions – Legendre polynomials.

UNIT IV RANDOM VARIABLES 10

One dimensional Random Variable - Moments and MGF – Binomial, Poisson, Geometrical, Normal Distributions- Two dimensional Random Variables – Marginal and Conditional Distributions – Covariance and Correlation Coefficient - Functions of Two dimensional random variable.

UNIT V QUEUING THEORY 10

Single and Multiple server Markovian queuing models - Steady state system size probabilities – Little's formula - Priority queues - M/G/1 queuing system – P.K. formula.

L+T: 50 +10=60

REFERENCES

1. Sankara Rao.K. "Introduction to Partial Differential Equation", PHI, 2nd edition 2006.
2. Taha. H.A., "Operations Research- An Introduction," 8th Edition, PHI, 2006.
3. Jain M.K. Iyengar, S.R.K. & Jain R.K., "International Methods for Scientific and Engineering Computation", New Age International (P) Ltd, Publishers 2003.
4. Kanpur J.N. & Saxena. H.C. "Mathematical Statistics", S.Chand & Co., New Delhi, 2003.
5. Greweal B.S. "Higher Engineering Mathematics", Khanna Publishers, 2005.

12AE12 STATISTICAL DIGITAL SIGNAL PROCESSING

L T P C
3 1 0 4

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 10

Discrete Random Processes- Ensemble averages, stationary processes, Autocorrelation and Auto covariance matrices. Parseval's Theorem – Wiener - Khintchine Relation- Power Spectral Density- Periodogram Spectral Factorization - Filtering random processes. Low Pass Filtering of White Noise - Parameter estimation: Bias and consistency.

UNIT II SPECTRUM ESTIMATION **10**

Estimation of spectra from finite duration signals - Non-Parametric Methods-Correlation Method - Periodogram Estimator - Performance Analysis of Estimators -Unbiased, Consistent Estimators- Modified periodogram - Bartlett and Welch methods - Blackman –Tukey method. Parametric Methods - AR, MA, ARMA model based spectral estimation - Parameter Estimation -Yule-Walker equations - solutions using Durbin's algorithm.

UNIT III LINEAR ESTIMATION **10**

Solutions of the Normal equations- Levinson - Durbin algorithms - Least mean squared error criterion – FIR Wiener filter and Wiener IIR filters.

UNIT IVLINEAR PREDICTION **10**

Linear prediction - Forward and backward predictions - Wiener filter for filtering and prediction- Discrete Kalman filter

UNIT V ADAPTIVE FILTERS **10**

FIR adaptive filters - adaptive filter based on steepest descent method – Widrow Hoff LMS adaptive algorithm - Normalized LMS. Adaptive channel equalization - Adaptive echo cancellation – Adaptive noise cancellation- Adaptive recursive filters (IIR) - RLS adaptive filters-Exponentially weighted RLS sliding window RLS.

L+T= 50+10 = 60

REFERENCES

1. Monson Hayes.H., "Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc., Singapore, 2002.
2. John Proakis.G., Dimitris Manolakis.G., "Digital Signal Processing" Pearson Education, 4th edition 2006.
3. John Proakis.G.., "Algorithms for Statistical Signal Processing", Pearson Education, 2002.
4. Dimitris Manolakis.G, "Statistical and Adaptive Signal Processing", McGraw Hill, Newyork, 2000.
5. Rafael Gonzalez .C, Richard Woods E., "Digital Image Processing", Second Edition, Pearson Education, Inc., 2004. (For Wavelet Transform Topic)
6. S. J. Orfanidis, Optimum Signal Processing , 2nd Ed., 2007 Republication Of The 1988 Mcgraw-Hill Edition

12AE13 ADVANCED DIGITAL SYSTEM DESIGN L T P C

3 1 0 4

UNIT I SEQUENTIAL LOGIC CIRCUITS **10**

Mealy machine, Moore machine, Trivial/Reversible/Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in fundamental and pulse mode.

UNIT II SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **10**

Analysis of clocked synchronous sequential Networks (CSSN), Modeling of CSSN-State table assignment and reduction – Design of CSSN-Design of iterative circuits- ASM Chart- ASM Realization.

UNIT III ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **10**

Analysis of Asynchronous sequential Circuits (ASC)-Flow table reduction -Races in ASC--State assignment- Problem and the Transition table-Design of ASC-Static and Dynamic hazards-Data synchronizers-Designing of Vending machine controller-Mixed operating mode Asynchronous circuits.

UNIT IV LOGICAL EFFORT **10**

Definition of logical effort, Method of logical effort, Deriving the method of logical effort - Minimizing delay along a path – Choosing the length of the path, Calculating the logical effort of gates – Grouping input signals – calculating logical effort – Asymmetric logic gates – Catalog of logic gates.

UNIT V PROGRAMMABLE LOGIC DEVICES **10**

Basic concepts, programming technologies, Programmable Logic Element(PLE),Programmable Logic Array(PLA),Programmable Array Logic(PAL),Structure of standard PLD's ,Complex PLD's(CPLD)-System design using PLD's-Design of combinational and sequential circuits using PLD's ,Programmable PAL device using PALASM ,Design of state machine using Algorithmic State Machines(ASM) chart as design tool, Introduction to Field Programmable Gate Arrays.

L+T=50+10=60

REFERENCES

1. Charles Roth Jr .H, "Digital System Design using VHDL" Thomson Learning, 2 nd Edition 2007.
2. John Yarbrough. M "Digital Logic applications and Design" Thomson Learning, 2001.
3. Donald G.Givone, "Digital Principles and Design", Tata McGraw Hill, 2002.
4. John M Yarbrough, "Digital Logic Applications and Design", Thomson Learning, 2001.
5. Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India, 2001.
6. Charles H Roth Jr, "Fundamentals of Logic Design", Thomson Learning, 2004.

12AE14 MICROCONTROLLERS AND INTERFACING L T P C 3 0 0 3

UNIT I MICROPROCESSOR ARCHITECTURE **9**

Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – Register file – Cache – Virtual memory and Paging – Segmentation – Pipelining – The instruction pipeline – Pipeline Hazards – Instruction level parallelism – Reduced Instruction Set – Computer Principles – RISC Versus CISC – RISC Properties – RISC Evaluation – On-chip register versus Cache Evaluation

UNIT II HIGH PERFORMANCE RISC ARCHITECTURE **9**

The ARM Architecture –ARM organization and implementation – ARM Register Set – ARM instruction set – Thumb instruction set – ARM-Thumb Interworking – Supervisor mode, exception and traps – CPU performance – CPU power consumption – Design with microprocessors – Development and Debugging.

UNIT III PROGRAMMING AND OPTIMIZING CODE FOR RISC ARCHITECTURES **9**

ARM Assembly Language Programming – Profiling and Cycle Counting – Instruction Scheduling – Register Allocation – Conditional Execution – Looping Constructs – Bit Manipulation – Efficient Switches – Handling Unaligned Data – ARM High Level Language Programming – C Loop-

ing Structures – Register Allocation – Function Calls – Pointer Aliasing – Inline Functions and Inline Assembly.

UNIT IV MICROCONTROLLER INTERFACING AND BUSES 9

I/O Addresses of Ports and Device Addresses – Interrupts and I/Os – Bus Arbitration: Daisy Chain, Network Oriented Arbitration, Bus Architecture Arbitration – Real World Interfacing examples with LCDs, ADC and DACs. Serial Bus Protocols – I2C Bus, CAN Bus, USB Bus, FireWire IEEE 1394. Advanced Serial High Speed Buses, PCI, Wireless and Mobile System Protocols – IrDA, Bluetooth, 802.11, Zigbee.

UNIT V PROGRAMMABLE SYSTEM ON CHIP 9

Programmable Embedded System-on-Chip – Structure of the PSoC, PSoC Architecture, Programming and development of the software-reconfigurable PSoC. PSoC Modules – PWM, UART, Amplifiers, Filters, ADCs, DACs. Debugging - On-chip JTAG, Serial Wire Debug, Serial Wire Viewer – Introduction to PSoC Designer and PSoC Creator Tools.

TOTAL: 45

REFERENCE BOOKS

1. Danial Tabak, "Advanced Microprocessors", McGraw Hill, 2nd Ed, 1995.
2. Sivarama P. Dandamudi, "Guide to RISC Processors for Programmers and Engineers", Published 2005, Springer Publishers.
3. Steve Furber, "ARM System on Chip Architecture", 2nd Ed, Published 2000, Addison Wesley Publishers.
4. David Seal, "ARM Architecture Reference Manual", 2nd Ed, Published 2001, Addison Wesley Publishers.
5. N. Sloss, D. Symes, C.Wright, "ARM System Developer's Guide, Designing and optimizing System Software" , Published 2004, Morgann Kaufmann Publishers.
6. Robert Ashby, " Designer's Guide to the Cypress PSoC",1st Ed. Published 2005, Elsevier Publishers.
7. Alex Doboli, Eddie H. Currie, "Introduction to Mixed-Signal, Embedded Design", 2nd Ed. Published 2011, Springer Publisher
8. Wayne Wolf, "Computers as Components - Principles of Embedded Computer System Design", Morgan Kaufmann Publisher, 2006.

12AE15 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS L T P C 3 0 0 3

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a pn junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 9

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV ANALOG MULTIPLIER AND PLL 9

Analysis of four quadrant and variable transconductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY **9**

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascade and MOS Active Cascade Operational Amplifiers.

TOTAL:45

REFERENCES

1.Gray, Meyer, Lewis, Hurst, —Analysis and design of Analog IC's, 4th Edition, Wiley International, 2002.
2. Behzad Razavi, —Design of Analog CMOS Integrated Circuits, S.Chand and company ltd, 2000.
3. Nandita Dasgupata, Amitava Dasgupta, Semiconductor Devices, Modelling and Technology, Prentice Hall of Indiapvt.ltd, 2004.

12AE16 CONSUMER ELECTRONICS L T P C 3 0 0 3

UNIT I AUDIO SYSTEMS **9**

Microphones: characteristics of microphones; types and applications of microphones: carbon, crystal, moving coil, ribbon, capacitor, electrets, lavalier, tie-clip, cordless. Loud Speakers: properties of loud speakers, types of loud speakers: crystal, electrostatic, electrodynamic, horn type; baffles and enclosures, multi speaker system: woofers, tweeters; crossover networks; impedance matching. Public Address System: planning, speaker matching, amplifiers, equalizers. Sound recording on magnetic tape: its principles, tape transport mechanism; CD system, Hi-Fi system.

UNIT II VIDEO SYSTEMS **9**

Colour TV and HDTV systems: standards, principles, block diagram; LCD, LED, PLASMA Systems, Electronic cameras, VCR, VCD, DVD players, Dolby noise reduction digital and analog recording. Digital projection systems (LCD, DLP, SVGA to UXGA system) Block diagram and principles of working of cable TV and DTH, cable TV using internet.

UNIT III HOME APPLIANCES AND PRINTERS **9**

Microwave Oven, Washing machine, Air conditioners, Refrigerators- Construction and working principles, Inkjet Printer, Laser Printer, Printer Controller, Concentric Interface, Signals from PC to Printer & Printer to PC.

UNIT IV POWER SUPPLIES AND OTHER SYSTEMS **9**

SMPS, UPS and Preventive Maintenance, Set Top Boxes, Remote controls, Scanners-Bar codes/Flat bed, Facsimile, Xerography, Extension to a dynamic copier, Digital Clocks working.

UNIT V COMPLIANCE **9**

Product safety and liability issues; standards related to electrical safety and standards related to fire hazards, e.g., UL and VDE. EMI/EMC requirements and design techniques for compliance, e.g. ESD, RF interference and immunity, line current harmonics and mains voltage surge.

TOTAL:45

REFERENCES
1. Bali S.P, “Consumer Electronics”, Pearson Education, 2007
2. R.G.Gupta, “Audio and Video Systems”, Tata McGraw Hill, 2010.
3. B.R.Gupta, “Consumer Electronics”, S.K.Kataria&Sons, 2011
4. K. Blair, Benson “Audio Engineering Hand book”, 2001
5. R.R Gulati, “Complete Satellite & Cable Television”, New age International Publisher, 2008

12AE17 ELECTRONICS DESIGN LABORATORY I

L T P C
0 0 3 2

List of Experiments :

1. System design using PIC Microcontroller –UART, LED interface
2. Implementation of Adaptive Filter.
3. Implementation of Periodogram.
4. Simulation of FIR, IIR and Wiener in Matlab.
5. Modeling of Sequential Digital system using VHDL
6. Design and Implementation of ALU using FPGA.
7. Simulation of NMOS and CMOS circuits using PSPICE.
8. System design using ARM Processor Programming.

12AE21 EMBEDDED SYSTEM DESIGN

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

Embedded system- characteristics of embedded system- categories of embedded system- requirements of embedded systems- challenges and design issues of embedded system- trends in embedded system- system integration- hardware and software partition- applications of embedded system- control system and industrial automation biomedical- data communication system-network information appliances- IVR systems- GPS systems.

UNIT II DEVELOPMENT OF SOFTWARE ARCHITECTURE **9**

Development of software architecture – simple round robin architecture- design and implementation of digital multimeter- round robin with interrupt architecture- implementation of communication bridge- function queue scheduling architecture- RTOS architecture.

UNIT III HARDWARE ARCHITECTURE **9**

LED/LCD interfacing. Case study of processor- 16 bit and 32 bit processor-DSP processor. Hardware architecture- block schematic of a typical hardware architecture- CPU-memory-I/O Devices- design with microprocessor development-ADC- DAC interfacing

UNIT IV EMBEDDED SYSTEM PLATFORM AND DEVELOPMENT TOOLS **9**

Inter process communication- UART-IEEE 1394-IRDA-USB-PCI development tools- EPROM ERASER-signature validator- accelerated design for video accelerator.

UNIT V OVERVIEW OF DESIGN TECHNOLOGIES **9**

Design methodologies and tools- designing hardware and software components- system analysis and architecture design- system integration- structural and behavioral description smart cards.

TOTAL: 45

REFERENCES

1. Wayne Wolf, “Computers as Components”, Morgan Kaufmann publishers, 2nd Edition, 2008
2. Jean J.Labrosse, “Embedded System Building Blocks”, CMP, 2nd Edition, 2000
3. Arnold berger, “Embedded System Design”, CMP books, 1st Edition, 2001
4. Narayan and Gong, “Specifications and Design of Embedded Systems”, Pearson education, 2nd Edition, 1999

12AE22 ASIC DESIGN TECHNIQUES

L T P C
3 0 0 3

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN **9**

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort – Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS **9**

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY **9**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX – Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING **9**

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR & POWER PLANNING, PLACEMENT AND ROUTING **9**

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow global routing - detailed routing - special routing - circuit extraction – DRC, Power Planning, Clock Rate Synthesis, Static Timing Analysis

TOTAL: 50

REFERENCES

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
4. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.

12AE23 VIRTUAL INSTRUMENTATION SYSTEMS

L T P C
3 0 0 3

UNIT I VIRTUAL INSTRUMENTATION 9

Historical perspective, advantages, blocks diagram and architecture of a virtual instrument, data-flow techniques, graphical programming in data flow, comparison with conventional programming. Development of Virtual Instrument using GUI, Real-time systems, Embedded Controller, OPC, HMI / SCADA software, Active X programming.

UNIT II PROGRAMMING TECHNIQUES 9

VIS and sub-VIS, loops and charts, arrays, clusters and graphs, case and sequence structures, formula nodes, local and global variables, string and file I/O, Instrument Drivers, Publishing measurement data in the web.

UNIT III DATA ACQUISITION BASICS 9

Introduction to data acquisition on PC, Sampling fundamentals, Input/output techniques and buses. ADC, DAC, Digital I/O, counters and timers, DMA, Software and hardware installation, Calibration, Resolution, Data acquisition interface requirements.

UNIT IV CHASSIS REQUIREMENTS 9

Common Instrument Interfaces: Current loop, RS 232C/ RS485, GPIB. Bus Interfaces: USB, PCMCIA, VXI, SCSI, PCI, PXI, Fire wire. PXI system controllers, Ethernet control of PXI. Networking basics for office & Industrial applications, VISA and IVI.

UNIT V TOOLSETS, DISTRIBUTED I/O MODULES 9

Application of Virtual Instrumentation: Instrument Control, Development of process database management system, Simulation of systems using VI, Development of Control system, Industrial Communication, Image acquisition and processing, Motion control.

TOTAL: 45

REFERENCES

1. Gary Johnson, Lab VIEW Graphical Programming, Second edition, McGraw Hill, Newyork, 2006.
2. Sumathi.S & P.Surekha, Labview based Advanced Instrumentation Systems, Springer 2007.
3. Lisa K. wells & Jeffrey Travis, Lab VIEW for everyone, Prentice Hall, New Jersey, 2002.
4. Kevin James, PC Interfacing and Data Acquisition: Techniques for Measurement, Instrumentation and Control, Newnes, 2000.

12AE24 DIGITAL CONTROL ENGINEERING

L T P C
3 1 0 4

UNIT I INTRODUCTION **9**

Overview of frequency and time response analysis and specifications of control systems - Digital Control systems – basic concepts of sampled data control systems – principle of sampling, quantization and coding – Reconstruction of signals – Sample and Hold circuits – Practical aspects of choice of sampling rate -Basic discrete time signals – Time domain models for discrete time systems.

UNIT II MODELS OF DIGITAL CONTROL DEVICES AND SYSTEMS **9**

Z domain description of sampled continuous time plants – models of A/D and D/A converters – Z Domain description of systems with dead time – Implementation of digital controllers – Digital PID controllers –Position, velocity algorithms – Tuning – Zeigler – Nichols tuning method.

UNIT III STATE VARIABLE ANALYSIS **9**

State space representation of discrete time systems – Solution of discrete time state space equation – State transition matrix – Decomposition techniques – Controllability and Observability – Multi variable discrete systems.

UNIT IV STABILITY ANALYSIS **9**

Mapping between S plane and Z plane- Jury's stability test - Bilinear transformation and extended Routh array- Root Locus Method – Liapunov Stability Analysis of discrete time systems.

UNIT V DESIGN OF DIGITAL CONTROL SYSTEM **9**

Z plane specifications of control system design – Digital compensator design – Frequency response method - State feedback – Pole placement design – State Observers – Digital filter properties – Frequency response – Kalman‘s filter.

TOTAL : 45

REFERENCES

1 Gopal M. ‗ Digital Control and State Variable methods‘, Tata Mc Graw Hill Publishing Company Ltd., New Delhi, India, 2003.
2 Kuo B.C. ‗ Digital Control Systems‘, Oxford University Press, Inc., 2003.
3 Ogata K. ‗Discrete Time Control Systems‘, Prentice Hall International, New Gercy, USA, 2002.

12AE25 ELECTRONICS DESIGN LAB II

L T P C
0 0 3 2

List of Experiments

1. System design using PLL
2. System design using CPLD/FPGA
3. Design using embedded micro controller- LCD interface
4. Model train controller using embedded micro controller
5. Simulation of Non adaptive Digital Control System using MATLAB control system toolbox
6. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox
7. Virtual instrumentation using Labview
8. ASIC design using tanner or cadence

12AE26 TECHNICAL SEMINAR-1

L T P C
0 0 2 1

The student will make atleast two technical presentations on current topics related to the specialization. The same will be assessed by a committee appointed by the college. The students are expected to submit a report at the end of the semester covering the various aspects of his/her presentation. A quiz covering the above will be held at the end of the semester.

12AE32 TECHNICAL SEMINAR-2

L T P C
0 0 2 1

The student will make atleast two technical presentations on current topics related to the specialization. The same will be assessed by a committee appointed by the college. The students are expected to submit a report at the end of the semester covering the various aspects of his/her presentation. A quiz covering the above will be held at the end of the semester.

12AE2A COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

L T P C
3 0 0 3

UNIT I REVIEW OF COMPUTER ARCHITECTURE **9**

Computer architecture evolution-Multiprocessors and Multicomputer – Multivector and SIMD computers – PRAM and VLSI models – Architectural development tracks – Conditions of parallelism – Program partitioning and scheduling – System interconnect architectures – Parallelism in Uniprocessor systems – Parallel computer structures.

UNIT II PROCESSOR AND MEMORY **9**

Advanced processor technology – Super scalar and vector processors – Memory hierarchy – Virtual memory technology – Cache memory organization – Shared memory organization – Principles of designing pipelined processors – Design of pipelined instruction unions.

UNIT III ARRAY PROCESSORS **9**

SIMD array processors – SIMD computer organizations – Masking and data routing mechanisms – SIMD interconnect networks – Barrel shifter and data manipulator – shuffle – Exchange and omega networks – Parallel algorithms for array processors – Associative array processing – Performance enhancement methods (SIMD computers).

UNIT IV MULTIPROCESSOR ARCHITECTURE AND MULTIPROCESSING CONTROL **9**

Functional structures (Loosely and tightly coupled multiprocessors) – multistage networks for multiprocessor operating system – inter process communication system – system deadlocks and protection – parallel algorithms for multiprocessors.

UNIT V PARALLEL PROGRAM DEVELOPMENT AND ENVIRONMENTS **9**

Parallel programming environments – software tools and environments – visualization and performance tuning – synchronization and multiprocessing model – shared variable program structures – message passing program development – mapping programs on multicomputers.

TOTAL:45

REFERENCES

1. Kai Hwang, “Advanced computer architecture (parallelism scalability programmability)”, Tata McGrawHill, 2009
2. Kai Hwang Faye’ A.Briggs, “Computer Architecture and Parallel Processing”, Tata McGraw Hill, 1996
3. Terence Fountain, Peter Kacsuk, De zso Sigma, “Advanced Computer Architectures (A design space approach)”, Pearson Education Asia, 1997

12AE2B DIGITAL IMAGE PROCESSING

L T P C
3 0 0 3

Unit I FUNDAMENTALS OF IMAGE PROCESSING **9**

Introduction - Steps in image processing systems - Image acquisition - Sampling and Quantization - Pixel relationships - Color fundamentals and models, File formats, Image operations - Arithmetic, Geometric and Morphological.

UNIT II IMAGE ENHANCEMENT **9**

Spatial Domain: Gray level Transformations - Histogram processing - Spatial filtering smoothing and sharpening. Frequency Domain: Filtering in frequency domain - DFT, FFT, DCT - Smoothing and sharpening filters - Homomorphic Filtering.

UNIT III IMAGE SEGMENTATION AND FEATURE ANALYSIS **9**

Detection of Discontinuities - Edge operators - Edge linking and Boundary Detection - Thresholding -

Region based segmentation - Morphological Watersheds - Motion Segmentation, Feature Analysis and Extraction.

UNIT IV MULTI RESOLUTION ANALYSIS AND COMPRESSIONS **9**

Multi Resolution Analysis: Image Pyramids - Multi resolution expansion - Wavelet Transforms. Image compression: Fundamentals - Models - Elements of Information Theory - Error free compression - Lossy Compression - Compression Standards.

UNIT V APPLICATIONS OF IMAGE PROCESSING **9**

Image classification - Image recognition - Image understanding - Video motion analysis – Image fusion - Steganography - Digital compositing - Mosaics - Color Image Processing.

TOTAL = 45

REFERENCES

1.Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", 2nd Edition, Pearson Education, 2003

2.Anil K. Jain, "Fundamentals of Digital Image Processing", Pearson Education, 2003

3.Milan Sonka, Vaclav Hlavac and Roger Boyle, "Image Processing, Analysis and Machine Vision", 2nd Edition, Thomson Learning, 2001

12AE2C ELECTRO MAGNETIC INTERFERENCE & COMPATIBILITY IN SYSTEM DESIGN

L T P C

3 0 0 3

UNIT I EMI ENVIRONMENT **9**

Introduction to EMI/EMC-Basics of electro Magnetic interference (EMI) Fundamentals of electromagnetic compatibility(EMC)-Radiation hazards Transients and other EMI sources Transients Electrostatics discharge(ESD)-Tempest- Lightning – Standards of EMI

UNIT II EMI COUPLING **9**

EMI from apparatus and circuits: Introduction-Electromagnetic emission-Appliances-noise from relays and switches-nonlinearities in circuits-Passive inter modulation-Cross talk in transmission lines-Transmission in power supply lines-Electromagnetic interference.

UNIT III EMI SPECIFICATION/STANDARDS AND MEASUREMENTS **9**

Units of specification-civilian standards and military standards. Basics of EMI measurements-EMI measurement tools-TEMcell-measurement using TEM cell-Reverberating chamber-GTEM cell-Anechoic chamber-Open area test site-RF absorbers-conducted interference measurements-conducted EMI from equipments-Experimental setup for measuring conducted EMI-Measurement of DM interferences.

UNIT IV EMI CONTROL TECHNIQUE **9**

Shielding technique-Filter techniques-Grounding techniques-Bonding techniques-Cable connectors and components-Isolation transformer-Transient suppressor

UNIT V EMC DESIGN OF PCB **9**

Designing for EMC: Introduction-Different techniques involved in designing for EMC-EMC guide lines for PCB designs-EMC design guide line for audio and control circuit design-EMC guide lines for

RF design-EMC guidelines for power supply design-Mother board designs and propagation delay performance models

TOTAL:45

REFERENCES

1. Bernhard Keiser"Principles of Electromagnetic Compatibility", Artech house, 3rd edition 1987.
2. Henry W.Ott "Noise reduction Techniques in Electronics systems", Johnwiley and sons . NewYork 1988.
3. DonWhite consultant incorporate-Handbook of EMI/EMC- Vol 1-1985
4. Clayton R. Paul "Introduction to EMC", Wiley & sons, 2006.
5. Sathyamurthy.S"Basics of Electro Magnetic Compatibility", Society of EMC Engineering's (India), 2003.
6. Kodali.V.P "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 2001.

12AE2D MULTIMEDIA COMPRESSION AND CODING TECHNIQUES

L T P C
3 0 0 3

UNIT I INTRODUCTION AND TEXT COMPRESSION 9

Special features of Multimedia – Graphics and Image Data Representations - Fundamental Concepts in Video and Digital Audio – Storage requirements for multimedia applications -Need for Compression - Taxonomy of compression techniques – Overview of source coding, source models, scalar and vector quantization theory – Evaluation techniques – Error analysis and methodologies.
Compaction techniques – Huffmann coding – Adaptive Huffmann Coding – Arithmetic coding – Shannon-Fano coding – Dictionary techniques – LZW family algorithms.

UNIT II AUDIO COMPRESSION 9

Audio compression techniques - μ- Law and A- Law companding. Frequency domain and filtering – Basic sub-band coding – Application to speech coding – G.722 – Application to audio coding – MPEG audio, progressive encoding for audio – Silence compression, speech compression techniques – Formant and CELP Vocoders

UNIT III IMAGE COMPRESSION 9

Predictive techniques – DM, PCM, and DPCM: Optimal Predictors and Optimal Quantization – Contour based compression – Transform Coding – JPEG Standard – Sub-band coding algorithms: Design of Filter banks – Wavelet based compression: Implementation using filters – EZW, SPIHT coders – JPEG 2000 standards - JBIG, JBIG2 standards.

UNIT IV VIDEO COMPRESSION 9

Video compression techniques and standards – MPEG Video Coding I: MPEG – 1 and 2 – MPEG Video Coding II: MPEG – 4 and 7 – Motion estimation and compensation techniques – H.261 Standard – DVI technology – PLV performance – DVI real time compression – Packet Video.

UNIT V MULTIMEDIA NETWORKING APPLICATIONS 9

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

TOTAL: 45

REFERENCES

1. Khalid Sayood: Introduction to Data Compression, Morgan Kauffman Harcourt India, 2nd Edition, 2000.
2. Yun Q.Shi, Huifang Sun: Image and Video Compression for Multimedia Engineering Fundamentals, Algorithms & Standards, CRC press, 2003.
3. Mark S.Drew, Ze-Nian Li: Fundamentals of Multimedia, PHI, 1st Edition, 2003.
4. Watkinson. J: Compression in Video and Audio, Focal press, London.1995.
5. Jan Vozer: Video Compression for Multimedia, AP Profes, NewYork, 1995
6. Hersent Gurle & petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003.

12AE2E OPTO ELECTRONICS

L T P C
3 0 0 3

UNIT I ELEMENTS OF LIGHT AND SOLID STATE PHYSICS **9**

Wave nature of light, Polarization, Interference, Diffraction, Light Source, review of Quantum Mechanical concept, Review of Solid State Physics, Review of Semiconductor Physics and Semiconductor Junction Device.

UNIT II DISPLAY DEVICES AND LASERS **9**

Introduction, Photo Luminescence, Cathode Luminescence, Electro Luminescence, Injection Luminescence, Injection Luminescence, LED, Plasma Display, Liquid Crystal Displays, Numeric Displays, Laser Emission, Absorption, Radiation, Population Inversion, Optical Feedback, Threshold condition, Laser Modes, Classes of Lasers, Mode Locking, laser applications.

UNIT III OPTICAL DETECTION DEVICES **9**

Photo detector, Thermal detector, Photo Devices, Photo Conductors, Photo diodes, Detector Performance.

UNIT IV OPTOELECTRONIC MODULATOR **9**

Introduction, Analog and Digital Modulation, Electro-optic modulators, Magneto Optic Devices, Acoustoptic devices, Optical, Switching and Logic Devices.

UNIT V OPTOELECTRONIC INTEGRATED CIRCUITS **9**

Introduction, hybrid and Monolithic Integration, Application of Opto Electronic Integrated Circuits, Integrated transmitters and Receivers, Guided wave devices.

TOTAL: 45

REFERENCES

1. Pallab Bhattacharya "Semiconductor Opto Electronic Devices", Prentice Hall of India Pvt., Ltd., New Delhi, 2006.
2. Jasprit Singh, "Opto Electronics – As Introduction to materials and devices", McGraw-Hill International Edition, 1998
3. S C Gupta, Opto Electronic Devices and Systems, Prentice Hal of India, 2005.
4. J. Wilson and J.Haukes, "Opto Electronics – An Introduction", Prentice Hall, 1995

12AE2F LOW POWER VLSI DESIGN

L T P C
3 0 0 3

UNIT I POWER DISSIPATION IN CMOS **9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

UNIT II POWER OPTIMIZATION **9**

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS **9**

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION **9**

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9**

Synthesis for low power –Behavioral level transforms- Software design for low power.

TOTAL: 45

REFERENCES

1 K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley, 2000.
2 Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer, 2002.
3 J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.
4 S.Y. Kung, H.J. White House, T. Kailath, —VLSI and Modern Signal Processing, Prentice Hall, 1985.
5 Jose E. France, Yannis Tsividis, —Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing, Prentice Hall, 1994.

12AE2G REAL TIME OPERATING SYSTEMS

L T P C
3 0 0 3

UNIT I REVIEW OF OPERATING SYSTEMS **9**

Basic Principles - System Calls - Files - Processes - Design and Implementation of processes - Communication between processes - Operating System structures.

UNIT II DISTRIBUTED OPERATING SYSTEMS **9**

Topology - Network types - Communication - RPC - Client server model - Distributed file system - Design strategies.

UNIT III REAL TIME MODELS AND LANGUAGES **9**

Event Based - Process Based and Graph based Models - Petrinet Models - Real Time Languages -

RTOS Tasks - RT scheduling - Interrupt processing - Synchronization - Control Blocks - Memory Requirements.

UNIT IV REAL TIME KERNEL **9**

Principles - Design issues - Polled Loop Systems - RTOS Porting to a Target - Comparison and study of RTOS VX works and µCOS - Case studies.

UNIT V RTOS APPLICATION DOMAINS **9**

RTOS for Image Processing - Embedded RTOS for voice over IP - RTOS for fault Tolerant Applications - RTOS for Control Systems.

TOTAL: 45

REFERENCES

1. Charles Crowley, "Operating Systems-A Design Oriented approach", McGraw Hill 2009
2. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 2001
3. Tanenbaum, "Distributed Operating Systems", Pearson Education
4. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", PHI 1999

12AE2H WIRELESS AND MOBILE COMMUNICATION

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

PCS Architecture – Cellular Telephony – Cordless telephony Mobility Management: Handoff – Roaming Management – Roaming Management under SS7– Roaming Management for CT2 Handoff Management:

DETECTION AND ASSIGNMENT: Handoff Detection – Strategies for Handoff Detection –Channel Assignment.

RADIO LINK TRANSFER: Link transfer types – Hard Handoff – Soft Handoff.

UNIT II NETWORK SIGNALING **9**

IS-41 Network Signaling: Signaling System No.7 – Interconnection and Message Routing – Mobility Management using TCAP – PCN / PSTN Call control using ISUP – Intersystem Handoff.

PACS Network Signaling: Network Elements – Network Interfaces – AIN / ISDN Internetworking – Registration – Call Origination – Call Termination – Intersystem Handoff – Feature Interactions

UNIT III GSM SYSTEM AND MOBILITY MANAGEMENT **9**

GSM System – GSM Architecture – Location tracking and Call Setup – Security – Data services – GSM Network Signaling

GSM Mobility Management: GSM Location Update – Mobility Databases – VLR Identification Algorithm – VLR Overflow Control.

UNIT IV GPRS AND WAP **9**

GPRS: GPRS Functional Groups – GPRS Architecture – GPRS Network Nodes – GPRS Interfaces – GPRS Procedures – GPRS Billing.

WAP: WAP model – WAP Gateway – WAP Protocols – WAP UAProf and Caching.

UNIT V 3G SERVICES AND WLL **9**

3G Mobile Services: W-CDMA and CDMA 2000 – Improvement on Core Network – Quality of Service – Wireless Operating System – 3G Systems

Wireless Local Loop: Architecture – WLL Technologies – WLL OAM Functions.

TOTAL : 45

REFERENCES

1. Yi-Bing Lin, Imrich Chlamtac, "Wireless and Mobile Network Architectures", Wiley, 1st Edition, 2000.
2. Kaveth Pahlavan, K.Prasanth Krishnamurthy, "Principles of Wireless Networks", Pearson Education Asia, 2002
3. Leon Garcia, Widjaja, "Communication Networks", Tata Mc Graw Hill, New Delhi, 2000.
4. William Stallings, "Wireless Communications and Networks", Prentice Hall, 2002.

12AE3A ADVANCED ROBOTICS AND AUTOMATION

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS **9**

Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS **9**

Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D'Alembert equations of motion.

UNIT IV ROBOT APPLICATONS **9**

Material Transfer & Machine Loading / Unloading General Consideration in robot material handling transfer applications – Machine loading and unloading. Processing Operations
Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

UNIT V ASSEMBLY AND INSPECTION **9**

Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.

TOTAL : 45

REFFERENCES

1. Fu, Gonazlez.K.S. R.C. and Lee, C.S.G., Robotics (Control, Sensing, Vision and Intelligence), McGraw Hill, 1987

2. Wesley.E, Snyder.R, Industrial Robots, “Computer Interfacing and Control”, Prentice Hall International Edition, 1988
3. Asada and Slotine, “Robot analysis and Control”, John Wiley and sons, 1986
4. Philippe Coiffet, “Robot technology” - Vol.II (Modelling and Control), Prentice Hall Inc., 1983
5. Groover.M.P. Mitchell, Weiss, “Industrial Robotics Technology Programming and Applications”, Tata McGraw Hill, 2008

12AE3B APPLIED CRYPTOGRAPHY AND DATA SECURITY

L T P C
3 0 0 3

UNIT I CONCEPTS AND PROTOCOLS **9**

Terminology – Steganography – Substitutional ciphers- Ceaser, Mono alphabetic, poly alphabetic, Hill , Vigenere , Playfair – Transposition ciphers- rail fence, One time pad Protocols-Key exchange, authentication, secret splitting, Secret sharing, Time stamping services, subliminal channel, Digital signature, proxy signature, group signature, bit commitment, Fair coin flips.

UNIT II CRYPTOGRAPHIC ALGORITHMS **9**

Algorithm types and modes- Over view of symmetric key cryptography- Data Encryption Standard (DES) - IDEA – RC4-RC5-Blow fish-AES

UNIT III ASYMMETRIC / PUBLIC KEY ENCRYPTION **9**

Number theory-Prime numbers-Fermat’s and Euler’s theorem – Testing for primality -The Chinese remainder theorem- Discrete logarithms, Public key crypto systems- requirements – applications – The RSA algorithm- Key management – Diffie Hellman key exchange- Elliptic curve cryptography.

UNIT IV HASH FUNCTIONS AND DIGITAL SIGNATURE **9**

Message authentication- requirements – functions – codes – Hash functions, Hash algorithms- MD5 message digest algorithm – Secure Hash algorithm – HMAC, Digital signature- Digital Signature Standard – DSS Approach – Digital Signature algorithm

UNIT V DATA SECURITY **9**

Internet security protocols- basic concepts – Secure socket layer(SSL)- transport layer security(TLS) – Secure HTTP – Time Stamping protocol – Secure electronic transaction (SET)- SSL Versus SET- Email security – WAP Security- Security in GSM – Security in 3G - Bio metric authentication – Kerberos- Single sign on (SSO) approaches.

TOTAL:45

REFERENCES

1. Bruce Schneier, “Applied Cryptography”, 2nd Edition, John Wiley & Sons
2. Atul Kahate, “Cryptography and Network Security”, 2nd Edition, Tata McGraw Hill, 2009
3. William Stallings, “Cryptography and Network Security”, 3rd Edition, Pearson Education, 2003
4. Douglas R Stinson, “Cryptography – Theory and Practice”, CRC press

12AE3C BLUETOOTH TECHNOLOGY

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

Introduction to Wireless technologies: WAP services, serial and parallel Communication, Asynchronous and synchronous communication, EDM, TFM, Spread spectrum technology. Introduction to Bluetooth: Specification, core protocols, cable replacement protocol.

UNIT II BLUETOOTH RADIO AND NETWORKING **9**

Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hopping Bluetooth Networking: Wireless networking, Wireless network types, devices roles and states, adhoc network, scatter net.

UNIT III CONNECTION ESTABLISHMENT PROCEDURE **9**

Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth Security, Security architecture, Security level of services, profile and usage model: Generic access profile (GAP),SDA,serial profile, Secondary Bluetooth profile.

UNIT IV HARDWARE **9**

Hardware: Bluetooth implementation, Baseband overview, packet format, Transmission Buffers, Protocol implementation: link manager protocol, logical link control Adaptation protocol, Host control interface, protocol interaction with layers.

UNIT V APPLICATIONS **9**

Programming with Java: Java Programming, J2ME architecture, Java x , Bluetooth package interface, classes, exceptions, Javax.obex package: interfaces, classes, Bluetooth services overview of IRDA, Home RF, Wireless LANs, JINI.

TOTAL=45

REFERENCES

1. C.S.R.Prabhu and A.P.Reddi, “Bluetooth Technology”, Prentice Hall of India, 2004.
2. Charels P.Pfleeger, “Security in computing”, Prentice Hall, 2003.
3. Andreas F.Molisch, “Wideband wireless Digital Communication”, Prentice Hall PTR, 2001.
4. George.V.Tsoulous, “Adaptive Antennas for wireless

12AE3D EMBEDDED COMMUNICATION SOFTWARE DESIGN

L T P C
3 0 0 3

UNIT I INTRODUCTION TO COMMUNICATION **9**

OSI Reference Model Communication Devices - Communication Echo System Design Consideration - Host Based Communication - Embedded Communication System - OS Vs RTOS.

UNIT II SOFTWARE PARTITIONING **9**

Limitation of strict Layering - Tasks & Modules - Modules and Task Decomposition -Layer2 Switch - Layer3 Switch / Routers - Protocol Implementation - Management Types - Debugging Protocols.

UNIT III TABLES & OTHER DATA STRUCTURES **9**

Partitioning of Structures and Tables - Implementation - Speeding Up access - Table Resizing - Table access routines - Buffer and Timer Management - Third Party Protocol Libraries.

UNIT IV MANAGEMENT SOFTWARE

9

Device Management - Management Schemes - Router Management - Management of Sub System Architecture - Device to manage configuration - System Start up and configuration.

UNIT V MULTI BOARD COMMUNICATION SOFTWARE DESIG

9

Multi Board Architecture - Single control Card and Multiple line Card Architecture - Interface for Multi Board software - Failures and Fault - Tolerance in Multi Board Systems - Hardware independent development - Using a COTS Board - Development Environment - Test Tools.

TOTAL = 45

REFERENCES

1.Sridhar .T, "Designing Embedded Communication Software", Elsevier publications, 2003
2.Data communication and networking by Behrouz a Forouzan 4th edition,Tata McGraw Hill, 2006.

12AE3E EMBEDDED CONTROL SYSTEMS

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

Controlling the hardware with software - Data lines - Address lines - Ports - Schematic representation - Bit masking - Programmable peripheral interface - Switch input detection - 74 LS 244.

UNIT II INPUT-OUTPUT DEVICES

9

Keyboard basics - Keyboard scanning algorithm - Multiplexed LED displays - Character LCD modules - LCD module display - Configuration - Time-of-day clock - Timer manager - Interrupts - Interrupt service routines - IRQ - ISR - Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

UNIT IIII D/A AND A/D CONVERSION **9**

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 - Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

UNIT IV ASYNCHRONOUS SERIAL COMMUNICATION **9**

Asynchronous serial communication - RS-232 - RS-485 - Sending and receiving data - Serial ports on PC - Low-level PC serial I/O module - Buffered serial I/O.

UNIT IV CASE STUDIES: EMBEDDED C PROGRAMMING

9

Multiple closure problems - Basic outputs with PPI - Controlling motors - Bi-directional control of motors - H bridge - Telephonic systems - Stepper control - Inventory control systems.

TOTAL = 45

REFERENCES

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C", the publisher, Paul Temme, 2000
2. Ball S.R., "Embedded microprocessor Systems - Real World Design", Prentice Hall,2002
3. Herma K, "Real Time Systems - Design for distributed Embedded Applications", Kluwer Academic, 2011
4. Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", PHI, 2002

12AE3F HIGH DEFINITION TELEVISION

L T P C
3 0 0 3

UNIT I INTRODUCTION TO CABLE TELEVISION AND ANALOG TELEVISION **9**

Technology – related regulatory issues – The development of Cable Television Industry and Its services – Cable network Design – Coaxial system limitation- Introduction of fiber optics.
Analog television: Base band Monochrome Video and Monaural Audio – Modulation – Modern Analog Television.

UNIT II HDTV AND COMPRESSED HISTORY OF HDTV **9**

Analog & Digital Television – Going Hidef – Broadcast Engineering & Information Technology.
The road to HDTV- the Grand Alliance – A DTV Standard at last – Producing HDTV – HD Goes coast – to – coast – DTV conversion.

UNIT III DTV FUNDAMENTALS AND DTV RECEIVER **9**

Engineering Basics – Presentation – Compression - MPEG – 2 – Video Compression – Audio compression – Compressed data streams – Packetized transport – Transmission.
Reception and Demodulation – Transport Stream Demultiplexing – Decoding and Decompression – Program Assembly and Presentation – Receiver Issues – Presentation concern.

UNIT IV DTV STANDARDS AND THE TRANSITION TO METADATA **9**

Standards Bodies – the ATCS standards – SMPTE standards – the audio engineering Society – cable DTV Standards.
The origins of meta data in Broadcasting – content related to metadata – control metadata.

UNIT V EMERGING TECHNOLOGIES AND DIGITAL BROAD CASTING **9**

Presentation – Compression – Delivery and Distribution – MPEG and Metadata enhanced - Interactive and personalized – virtual product placement – Multiemergency alert system.
Digital broadcasting technology- consumers and DTV availability- global transition

TOTAL: 45

REFERENCES

1.HDTV and Transition to Digital Broadcasting, Philip J. Cianci, Focal press – 2007
2.Modern cable television technology , Video, voice and data communications, Walter ciciora, James farmer, david large, Michael adams, Second Edition

12AE3G HIGH PERFORMANCE COMMUNICATION NETWORKS

L T P C
3 0 0 3

UNIT I PACKET SWITCHED NETWORKS **9**

OSI and IP models, Ethernet (IEEE 802.3), Token ring (IEEE 802.5), FDDI, DQDB, SMDS: Internetworking with SMDS.

UNIT II ISDN AND BROADBAND ISDN **9**

ISDN - overview, interfaces and functions, Layers and services - Signaling System 7 - Broadband ISDN architecture and Protocols.

UNIT III ATM AND FRAME RELAY **9**

ATM: Main features-addressing, signaling and routing, ATM header structure-adaptation layer, management and control, ATM switching and transmission.
Frame Relay: Protocols and services, Congestion control, Internetworking with ATM, Internet and ATM, Frame relay via ATM.

UNIT IV ADVANCED NETWORK ARCHITECTURE **9**

TCP/IP - Architectures – Address mapping-IPv6- IGMP-ICMPv6- Multicasting -Resource Reservation Protocol (RSVP)- Differentiated services.

UNIT V WIRELESS NETWORKS **9**

Wireless LAN (IEEE 802.11) – Infrared LAN-Spread spectrum LAN-Architecture- Ad hoc networks-Blue tooth -Protocol stack.

TOTAL: 45

REFERENCES

1. William Stallings , “ISDN and Broadband ISDN with Frame Relay and ATM”, 4th edition, Pearson education Asia, 2002.
2. Leon Gracia, Widjaja, “Communication networks ", Tata McGraw-Hill, New Delhi, 2000.
3. William Stallings, “Wireless Communications and Networking”, PHI, 2004
4. Jennifer Bray and Charles F.Sturman, “Blue Tooth” Pearson education Asia, 2001.
5. Sumit Kasera, Pankaj Sethi, “ATM Networks ", Tata McGraw-Hill, New Delhi, 2000.
6. Rainer Handel, Manfred N.Huber, Stefan Schroder, “ATM Networks”,3rd edition, Pearson education asia,2002.
7. Jean Walrand and Pravin varaiya, “High Performance Communication networks”, 2nd edition, Harcourt and Morgan Kauffman, London 2000.
8. Behrouz A. Forouzan, “Data Communication and Networking’’, Tata McGraw Hill, 4th edition,2005

12AE3H INTERNET TECHNOLOGIES AND APPLICATIONS

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

Introduction to course: Review networking concepts (Basics of Computer communication and networking - LAN, WAN etc.)

UNIT II INTERNET CORE **9**

Internet core - Fundamental Protocols (IP, TCP, UDP, ICMP, ARP and an introduction to IP multicast) - IP routing and Routing protocols (RIP, RIP -II, IGRP, EIGRP, OSPF etc.) - TCP and UDP in more depth; IP network design and troubleshooting. The Domain Name System (DNS), DHCP, and other Important IP Utility Protocols.

UNIT III INTERNET APPLICATIONS

9

Internet applications - Fundamental Applications (Email, Telnet, File Transfer, and News) - Directories & Distributed Applications (NFS, LDAP, ILS, NIS etc.). Internet applications - Streaming & Real time communications (H.323 VTC, VolP, Netmeeting etc.).

UNIT IV WORLD WIDE WEB

9

The World Wide Web Part 1 - The basics (HTML, HTTP and security protocols) The World Wide Web Part 2 - Advanced topics (CGI, Perl, D-HTML, Java, ASP, VRML & SML)

UNIT V INTERNET MANAGEMENT & SECURITY **9**

SNMP, RMON, IPsec, L2TP, and others. The future of the Internet & Related applications - IPv6, Internet2, and NGI. Some hardwork assignments will require the use of common network troubleshooting tools, retrieval of information from the web, and basic Web-related programming assignments. (Typically Linux systems should be sufficient. Any LAN can be converted into a Linux LAN).

TOTAL: 45

REFERENCES

1. Computer networking - A top down approach featuring the internet James F. Kurose and Keith W Ross (Pearson Addison Wesley).
2. Stevens, —Unix Network Programming, Vol.1, Second Edition, Prentice Hall, 2004.
3. Stevens, —Unix Network Programming, Vol.2, Second Edition, prentice Hall, 2002.
4. Internetworking with TCP/IP Volume I: Principles, protocols, Architecture by Dougles E. Corner.

12AE3I MICRO ELECTRO MECHANICAL SYSTEMS

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

Intrinsic Characteristics of MEMS – Energy Domains and Transducers- Sensors and Actuators – Introduction to Micro fabrication - Silicon based MEMS processes – New Materials – Review of Elec-

trical and Mechanical concepts in MEMS – Semiconductor devices – Stress and strain analysis – Flexural beam bending- Torsional deflection.

UNIT II SENSORS AND ACTUATORS **9**

Electrostatic sensors – Parallel plate capacitors – Applications – Interdigitated Finger capacitor – Comb drive devices – Thermal Sensing and Actuation – Thermal expansion – Thermal couples – Thermal resistors – Applications – Magnetic Actuators – Micro magnetic components – Case studies of MEMS in magnetic actuators.

UNIT III SENSORS AND ACTUATORS **9**

Piezoresistive sensors – Piezoresistive sensor materials - Stress analysis of mechanical elements – Applications to Inertia, Pressure, Tactile and Flow sensors – Piezoelectric sensors and actuators – piezoelectric effects – piezoelectric materials – Applications to Inertia , Acoustic, Tactile and Flow sensors.

UNIT IV MICROMACHINING **9**

Silicon Anisotropic Etching – Anisotropic Wet Etching – Dry Etching of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case studies - Basic surface micromachining processes – Structural and Sacrificial Materials – Acceleration of sacrificial Etch – Striction and Antistriction methods – Assembly of 3D MEMS – Foundry process.

UNIT V POLYMER AND OPTICAL MEMS **9**

Polymers in MEMS– Polimide - SU-8 - Liquid Crystal Polymer (LCP) – PDMS – PMMA – Parylene – Fluorocarbon - Application to Acceleration, Pressure, Flow and Tactile sensors- Optical MEMS – Lenses and Mirrors – Actuators for Active Optical MEMS.

TOTAL: 45

REFERENCES

1. Chang Liu, 'Foundations of MEMS', Pearson Education Inc., 2006.
2. James J.Allen, micro electro mechanical system design, CRC Press published in 2005
3. Nadim Maluf, "An introduction to Micro electro mechanical system design", Artech House, 2000.
4. Mohamed Gad-el-Hak, editor, "The MEMS Handbook", CRC press Baco Raton, 2000
5. Tai Ran Hsu, "MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.
6. Julian w. Gardner, Vijay k. varadan, Osama O.Awadelkarim,micro sensors mems and smart devices, John Wiley & son LTD,2002

12AE3J NANO ELECTRONICS

L T P C
3 0 0 3

UNIT I INTRODUCTION TO NANOTECHNOLOGY **9**

Background to nanotechnology: Types of nanotechnology and nanomachines – periodic table – atomic structure – molecules and phases – energy – molecular and atomic size – surface and di-

mensional space – top down and bottom up; Molecular Nanotechnology: Electron microscope – scanning electron microscope – atomic force microscope – scanning tunnelling microscope – nanomanipulator – nanotweezers – atom manipulation – nanodots – self assembly – dip pen nanolithography. Nanomaterials: preparation – plasma arcing – chemical vapor deposition – sol-gels – electro deposition – ball milling – applications of nanomaterials.

UNIT II FUNDAMENTALS OF NANOELECTRONICS **9**

Fundamentals of logic devices:- Requirements – dynamic properties – threshold gates; physical limits to computations; concepts of logic devices:- classifications – two terminal devices – field effect devices – coulomb blockade devices – spintronics – quantum cellular automata – quantum computing – DNA computer; performance of information processing systems;- basic binary operations, measure of performance processing capability of biological neurons – performance estimation for the human brain. Ultimate computation:- power dissipation limit – dissipation in reversible computation – the ultimate computer.

UNIT III SILICON MOSFETs & QUANTUM TRANSPORT DEVICES **9**

Silicon MOSFETS - Novel materials and alternate concepts:- fundamentals of MOSFET Devices- scaling rules – silicon-dioxide based gate dielectrics – metal gates – junctions & contacts – advanced MOSFET concepts. Quantum transport devices based on resonant tunneling:- Electron tunneling – resonant tunneling diodes – resonant tunneling devices; Single electron devices for logic applications:- Single electron devices – applications of single electron devices to logic circuits.

UNIT IV CARBON NANOTUBES **9**

Carbon Nanotube: Fullerenes - types of nanotubes – formation of nanotubes – assemblies – purification of carbon nanotubes – electronic properties – synthesis of carbon nanotubes – carbon nanotube interconnects – carbon nanotube FETs – Nanotube for memory applications – prospects of an all carbon nanotube nanoelectronics.

UNIT V MOLECULAR ELECTRONICS **9**

Electrodes & contacts – functions – molecular electronic devices – first test systems – simulation and circuit design – fabrication; Future applications: MEMS – robots – random access memory – mass storage devices.

TOTAL: 45

REFERENCES

1. Michael Wilson, Kamali Kannangara, Geoff Smith, Michelle Simmons and Burkhard Raguse, Nanotechnology: Basic Science and Emerging Technologies, Chapman & Hall / CRC, 2002
2. T. Pradeep, NANO: The Essentials – Understanding Nanoscience and Nanotechnology, TMH, 2007
3. Rainer Waser (Ed.), Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley-VCH, 2003

12AE3K PC BASED INSTRUMENTATION CONTROL

L T P C
3 0 0 3

UNIT I INTRODUCTION **9**

Review of microprocessors, microcomputers, micro processing systems - Input-output structures - Measurement of digital computer power and performance.

UNIT II DIGITAL CONTROL **9**

Need for computer in a control system – Functional Block Diagram of a Control system – Direct digital Control – Supervisory Control – Digital Control Interfacing: Process input, Output interface, Types of Display, Computer various inputs / output – Computer Control Action – Treatment of inputs, Outputs, Control Strategies – SCADA

UNIT III INTERFACING **9**

Analogue signal conversion – Interface components and techniques - Signal processing - Interface systems and standards – Communications.

UNIT IV SOFTWARE **9**

Real time languages – Programming real time systems - Discrete PID algorithms -Real time operating systems - Case studies in instrumentation.

UNIT V APPLICATION EXAMPLES IN MEASUREMENT AND CONTROL **9**

PC based data - Acquisition systems - Industrial process measurements, like flow temperature, pressure, and level PC based instruments development system.

TOTAL : 45

REFERENCES

1. Ahson, S.I., "Microprocessors with applications in process control", Tata McGraw Hill Publishing Company Limited, New Delhi, 1984.
2. George Barney C., "Intelligent Instrumentation", Prentice Hall of India Pvt. Ltd., New Delhi, 1998.
3. Krishna Khant, "Computer based industrial control", Prentice Hall, 1997.

12AE3L RF SYSTEM DESIGN

L T P C
3 0 0 3

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES **9**

CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link

Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct up conversion, two step up conversion

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS **9**

S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS **9**

Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation Power Amplifiers: General model –

Class A, AB, B, C, D, E and F amplifiers – Linearization Techniques – Efficiency boosting techniques – ACPR metric – Design considerations

UNIT IV PLL AND FREQUENCY SYNTHESIZERS **9**

PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers

UNIT V MIXERS AND OSCILLATORS **9**

Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – subsampling mixers Oscillators: Describing Functions , Colpitts oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise

TOTAL: 45

REFERNCES

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004
2. B.Razavi, “RF Microelectronics”, Pearson Education, 2011
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 2010
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.

12AE3M RFID AND ITS APPLICATIONS

L T P C
3 0 0 3

UNIT I RF Fundamentals **9**

RF operating principle – Frequency divider –Coupling – Inductive coupling, Electromagnetic back scatter coupling, close coupling, Electrical coupling – Frequency ranges used in RF Coding - Digital Modulation – ASK,FSK,PSK.

UNIT II RFID System Principles **9**

RFID systems – Component of an RFID System – Frequency, Range & Coupling – Transponder & Reader System – Equivalent Circuit – RFID Antennas: Antenna Parameters – Gain & directional effect, EIRP & ERP, Input impedance, Effective aperture and scatter aperture, Effective length. Antenna types – Dipole antennas, Yagi – Uda Antenna, Patch or micro strip antenna, Slot antennas

UNIT III RFID System Architecture **9**

Architecture of Transponder – HF interface, Address & Security logic, Memory architecture Microprocessors. Architecture of Reader - Components, Control Unit, Example – Reader IC U2270B, Connection of Antennas for inductive systems.

UNIT IV RFID Middleware for Applications **9**

Motivations – Logical Architecture – Application Level Events Specification – Commercial RFID Middleware – Example

UNIT V RFID Applications **9**

Example Applications – Contact less Smart Cards, Public Transport, Ticketing, Access Control, Transport Systems, Animal Identification. Electronic immobilization, Container Identification, Waste Disposal, Industrial Automation, Medical Applications

TOTAL: 45

REFERENCES

1. K.Finkenzeller, RFID Handbook: Fundamentals and Applications in contact less smart cards and identifications, John Wiley and sons Ltd, 2003
2. Bill Glover and Himanshu Bhatt, RFID Essentials, Oreilly, 2006.
3. Patrick J.Sweeney II, RFID for Dummies, Wiley Publishing, Inc.
4. Sandip Lahiri, RFID Handbook, IBM, 2006.