About the Institution

P.S.R. Engineering College is an Autonomous Institution established in the year 1999 by P.S.Ramasamy Telugu Minority Educational and Charitable Trust, towering high in quality of academic excellence and developments. It strives hard to achieve excellence by revamping research and extension activities, academic flexibility, publications in peer reviewed journals and modern laboratory facilities. The college received Education Excellence award for "Best Engineering College for Academic Infrastructure" in South Tamilnadu by Education post in 2013. The institution achieved tenth among all the Autonomous Institution under Anna University in Examinations. National Board of Accreditation(NBA) has accredited four UG programmes — ECE, CSE, EEE & MECH under Tier-I Category and also Accredited by National Assessment and Accreditation Council (NAAC) with A+ Grade. The institute offers academic programs with innovative curriculum, advanced research and societal engagement through outreach activities. The institute has 9 UG programmes, 6 PG programmes including MBA Programme and 7 Ph.D. programmes.

About the Department

The Department of Electronics and Communication Engineering is functioning since the inception of the College. The department offers UG - ECE and PG - Applied Electronics. The Department aims to impart quality education with strong fundamentals to produce graduates with sound knowledge for the betterment of society and to meet the dynamic demands of industry. The benchmark features have helped the department to acquire NBA Accreditation since 2009 onwards. The department has IEEE, IETE and ISTE chapters. It encompasses the modern facilities, latest equipment's and software in various laboratories like VLSI Design, Embedded Systems, Communication Engineering, Digital Signal Processing and Electronics System Design Laboratories. The department has a Centre of Excellence on IOT and Robotics. The Department is recognized as Research Centre by Anna University for Ph.D. Programme. The Department has research grants, from various Government organized schemes like DST, AICTE and TNSCST.

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AICTE Training and Learning (ATAL) Sponsored

One Week

Faculty Development Programme on

Analog and Digital Design Flow for SoC Design and Application

27.11.2023 to 02.12.2023

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An Autonomous Institution, Approved by AICTE, New Delhi
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Objectives of AICTE ATAL FDP

The objectives of AICTE Training and Learning (ATAL) Academy are: To set up an Academy which will plan and help in imparting quality technical education in the country. To support technical institutions in fostering the research innovation and entrepreneurship through training. To stress upon empowering technical teachers & technicians using Information and Communication Technology. To utilize SWAYAM platform and other resource for the delivery of trainings. To provide a variety of opportunities for training and exchange of experiences. Such as workshops, orientations, learning communities, peer mentoring and other faculty development programmes. To support policy makers for incorporating training as per requirements.

About the Programme

In VLSI design, SoCs are typically designed using a combination of hardware and software components, including processors, memory, I/O interfaces, and other peripherals. These components are integrated onto a single chip using a combination of standard cell-based design and custom layout techniques. Design flow of SoC aims in the development of hardware and software of SoC designs. In general, the design flow of SoCs consists of: Hardware and Software Modules: Hardware blocks of SoCs are developed from pre-qualified hardware elements and software modules integrated using software development environment.

Topics to be covered

- MOSFET Characterization & Inverter Design
- Adiabatic Logic Circuit and its Applications
- MOS Amplifier Design an Intuitive Approach
- Common Source, Common Drain, Common Gate Amplifiers using current mirrors
- Analysis of SSA – DC Analysis, Transient Analysis and AC Analysis
- Introduction to Semi- custom IC Design
- Introduction to UART Design and Prospect
- Introduction to Full Custom IC Design (Cadence EDA tools)
- Hands on Lab: Cadence EDA Tools for RTL-GDSII
- Functional Verification, RTL Synthesis of Combinational and Sequential Circuits and FPGA Implementation
- Hands on Lab: RTL Design of UART Design
- Introduction to IC PPA Analysis, Timing and Power Analysis
- FPGA implementation of UART in Xilinx Vivado
- Leon Processor Architecture and Design

Resource Persons

Eminent Speakers from IITs, NITs, Reputed Institutions and Industrial Personalities will handle the sessions.

Registration Details

Participants may register for this course using the link https://www.aicte-india.org/atal

Target Audience

- The faculty members of the AICTE approved institutions, research scholars, PG Scholars, participants from Government, Industry etc. and faculty of host institutions.
- Registrations accepted will be based on first come first serve basis
- Test shall be conducted at the end of the program and participants will be awarded a certificate of participation by ATAL Academy.
- The certificate shall be issued to those participants who will have minimum 80% attendance and will score minimum 60% marks in the test.
- E-certificate will be provided by ATAL Academy after successful completion of FDP

Programme Schedule - 27.11.2023 to 02.12.2023

Dates	9.30 AM to 12.00 PM (Session – 1)	12.00 PM to 1.00 PM (Session – 2)	2.00 PM to 4.30 PM (Session – 3)	4.30 PM to 5.30 PM (Session – 4)
27.11.23	Inaugural Function/ MOSFET Characterization & Inverter Design	Article-1 discussion "Trending IC design directions in 2022." Journal of Semiconductors (2022)	Adiabatic Logic Circuit and its Applications	
28.11.23	MOS Amplifier Design an Intuitive Approach	Design of Single-stage Amplifier using Cadence Virtuoso tool (Case Study – Amplifier)	Common Source, Common Drain, Common Gate Amplifiers using current mirrors. Analysis of SSA – DC analysis, Transient Analysis and AC Analysis	
29.11.23	Introduction to Semi- custom IC Design	Introduction to UART Design and Prospect	Introduction to Full Custom IC Design (Cadence EDA tools)	Hands on Lab: Cadence EDA Tools for RTL-GDSII
30.11.23	Functional Verification	RTL Synthesis of Combinational and Sequential Circuits and FPGA Implementation	Hands on Lab: RTL Design of UART Design	
01.12.23	Introduction to IC PPA Analysis	Timing and Power Analysis	Industrial Visit	
02.12.23	Leon Processor Architecture and Design	Article-2 discussion - “Improving performance of the LEON architecture”. Microelectronic Journal (2022),	FPGA implementation of UART in Xilinx Vivado	