**P.S.R. ENGINEERING COLLEGE SIVAKASI-626 140**



(An Autonomous Institution, Affiliated to Anna University, Chennai)

 **QUESTION BANK**

|  |  |  |  |
| --- | --- | --- | --- |
| Programme: | B.E. | Branch | Electronics and Communication Engineering |
| Acad. Year: | 2018-2019 | Year/Semester | IV /VII  |
| Course Code: | 12EC72 | Course Name | **DSP Architecture and its Applications** |
| Course Tutor(s): | Ms.M.Indhu Mathi AP/ECE & Mr.R.senthil Ganesh AP/ECE |

**UNIT-I ADSP 21XX ARCHITECTURE AND PROGRAMMING**

**PART - A**

|  |  |
| --- | --- |
|  | What is the advantage of twos complement format? |
|  | How the IEEE format differs from two word format? |
|  | Find the 2’s complement of +72. |
|  | Compare IEEE floating point format with 1.15 fixed point format. |
|  | Define uniform random generation. |
|  | List the assembly instructions in ADSP 2100 for ALU. |
|  | Compare fixed point and floating point processors. |
|  | What is the algorithm for floating point addition? |
|  | Define Barrel shifter. |
|  | Distinguish between the approximation of sine and arc tangent functions. |

**PART – B**

|  |  |  |
| --- | --- | --- |
|  | Explain the architecture of ADSP 2100 processor. | 16 |
|  | i) Illustrate the concept of development system in ADSP 2100. | 6 |
| ii) Explain in brief Non-restoring Add/Subtract division algorithm with an example. | 10 |
|  | Elaborate the multi precision fixed point multiplication concept in DSP processor. | 16 |
|  | Develop ALP for multi precision division using ADSP 2100 processor. | 16 |
|  | i) Compare the features of ADSP 2100 and 2101 processors.  | 8 |
| ii) Explain the architecture of ADSP 2101 processor. | 8 |
|  | Develop Assembly Language Program for single-precision fixed point division in ADSP 2100 with explanation and diagram. | 6 |

**UNIT-II FFT AND FILTER IMPLEMENTATION USING ADSP 21XX**

**PART - A**

|  |  |
| --- | --- |
|  | Define decimation and interpolation. |
|  | What is block floating point scaling?  |
|  | Differentiate FIR and IIR filters.  |
|  | Compare the radix-2 DIT FFT & radix-2 DIF FFT. |
|  | Show the basic butterfly diagram of radix-2 DIT FFT. |
|  | List the equations for DIF-FFT. |
|  | What is dual node spacing? |
|  | List the applications of multirate filters. |
|  | Distinguish between stage loop and group loop. |
|  | What is meant by leakage and how it can be reduced? |

**PART - B**

|  |  |  |
| --- | --- | --- |
|  | Explain about multi rate filters and their implementation in ADSP 2100. | 16 |
|  | Illustrate the implementation of Radix-2 DIT FFT in ADSP2100 with ALP. | 16 |
|  | Explain the implementation of single and double precision FIR filters.  | 16 |
|  | Illustrate the implementation of two types of IIR filters. | 16 |
|  | i) Develop Radix-2 DIF-FFT equations. | 8 |
| ii) Develop ALP for implementation of Butterfly loop in DIF FFT. | 8 |

**UNIT-III TMS320C6X ARCHITECTURE**

**PART - A**

|  |  |
| --- | --- |
|  | Define velociTI. |
|  | List the linker command file. |
|  | Define reset initialization code. |
|  | What is meant by non-maskable interrupt? |
|  | Compare the operation of pipelined CPU and non-pipelined CPU. |
|  | Distinguish between VLIW and velociTI. |
|  | List the special purpose instructions of C64x processor. |
|  | Distinguish little-endian and big-endian format. |
|  | What are the C6x software tools? |
|  | Define IDE. |

**PART - B**

|  |  |  |
| --- | --- | --- |
|  | Interpret the architecture of TMS320C6x architecture with explanation. | 16 |
|  | Explain about C6x DSK/EVM Target boards and assembly file. | 16 |
|  | i) Elaborate memory management and compiler utility in C6x processors. | 8 |
| ii) Discuss about interrupt data processing. | 8 |
|  | Demonstrate the architecture of TMS320C54x processor. | 16 |
|  | Outline the concepts of CPU operation in TMS320C6x processor with an example. | 16 |

**UNIT-IV CODE OPTIMIZATION**

**PART - A**

|  |  |
| --- | --- |
|  | List the types of cross path. |
|  | What is meant by software pipelining? |
|  | Define code optimization. |
|  | List C64x improvements. |
|  | What are the three stages of hand coded software pipelining? |
|  | Define circular buffering. |
|  | What is the general syntax of a linear assembly code line?  |
|  | Identify the applications of adaptive filtering. |
|  | Outline the dependency graph terminology. |
|  | List the linear assembly directives. |

**PART - B**

|  |  |  |
| --- | --- | --- |
|  | Explain about software pipelining. | 16 |
|  | i) Discuss about circular buffering. | 8 |
| ii) Analyze the hand coded software pipelining with example. | 8 |
|  | i) Elaborate word wide optimization in processor. | 6 |
| ii) Construct code optimization by mixing C and assembly. | 10 |
|  | Demonstrate the implementation of real time filters with suitable example. | 16 |
|  | Outline the concept of adaptive filtering and how it is implemented in C6x processor? | 16 |

**UNIT-V FRAME PROCESSING, REAL TIME ANALYSIS AND SCHEDULING**

**PART - A**

|  |  |
| --- | --- |
|  | What is meant by real time scheduling? |
|  | How will you monitor CPU load? |
|  | List the DSP/BIOS features available in CCS. |
|  | Define Soft real time. |
|  | List the types of real time constraints. |
|  | What is triple buffering technique? |
|  | Distinguish between DMA and EDMA. |
|  | What is real time data exchange? |
|  | What is the feature of execution graph window? |
|  | Define multithread scheduling. |

**PART - B**

|  |  |  |
| --- | --- | --- |
|  | Explain about real-time analysis and scheduling. | 16 |
|  | i) Elaborate the concept of DMA with neat diagram. | 8 |
| ii) Outline the concept of EDMA. | 8 |
|  | Discuss about Direct Memory Access and DSP Host communication. | 16 |
|  | Develop C programs for real time implementation of DFT and FFT in C6x processor. | 16 |
|  | Explain about data synchronization and communication. | 16 |