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**QUESTION BANK**

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| Programme: | B.E. | Branch | Electronics and communication Engg. |
| Academic Year: | 2018-2019 | Year/Semester | II Yr/ III Sem |
| Course Code: | 161EC32 | Course Name | Digital Electronics |
| Course Tutor(s): | Mr.G.LINGASAMY, AP/ECE, Mr.S.ATHIMOOLAM,AP/ECE |

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| **UNIT I -- NUMBER SYSTEM & MINIMIZATION TECHNIQUES** |  |
| **PART – A (2 Marks)** |  |
| 1 | Define Digital circuits. |  |
| 2 | Convert the decimal number 24.775 in to its equivalent binary number |  |
| 3 | Convert (A2B)16 in to its equivalent Octal umber |  |
| 4 | Subtract 1101 from 1011 by using 2’s complement method. |  |
| 5 | Subtract 1001 from 1110 by using 1’s complement method. |  |
| 6 | State De-Morgan’s Theorem |  |
|  7 | State Consensus Theorem |  |
| 8 | List the binary codes |  |
| 9 | What is error detection and correction code? |  |
| 10 | Define Canonical form of Boolean function. |  |
| 11 | Define Minterm and Maxterm. |  |
| 12 | What is the purpose of simplifying the Boolean function? |  |
| 13 | Compare the K-Map method with Queen Mc-Cluskey method |  |
|  | **PART-B**  |  |
| 1. | i) Simplify the Boolean fn   | (6) |
|  | ii) Simplify the following Boolean function by using K-Map method F(A,B,C,D,E) = ∑m(0,2,5,7,8,10,13,15,21,23,27,31 ) + ∑d(26,29 ) | (10) |
| 2 | i)Simplify the Boolean function  | (6) |
|  | ii) Simplify the following Boolean function by using K-Map method F(A,B,C,D,E) = ∑m(2,4,5,9,12,13,20, 22,23,25,28,29, 31 ) + ∑d(21,30 ) | (10) |
| 3 | i)Construct the circuit diagram for the boolean function  by using only NAND Gates | (8) |
|  | ii) Simplify the following Boolean function by using K-Map method F(A,B,C,D) = ∑m( 5,6,7,12,13) + ∑d(4,9,14,15 ) | (8) |
| 4 | i)Construct the circuit diagram for the boolean function by using only NOR Gates | (8) |
|  | ii) Implement the NAND gates for all other gate’s functions | (8) |
| 5 | Simplify the following Boolean function by using Queen Mc-Cluskey method  F(A,B,C,D) = ∑m(1,2,3,5,9,12,14,15) + ∑d(4,8,11 ) | (16) |
| 6 | Simplify the following Boolean function by using Queen Mc-Cluskey method F(A,B,C,D) = ∑m(0,2,3,6,7,8,10,12,13 ) | (16) |
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|  | **UNIT II-- LOGIC GATES & COMBINATIONAL CIRCUITS** |  |
|  | **PART – A (2 Marks)** |  |
| 1 | What is Combinational circuit? |  |
| 2 | List is logic families |  |
| 3 | What are Universal gates? Why these are called so? |  |
| 4 | Implement OR gate by using only NAND gates. |  |
| 5 | Implement AND gates by using only NOR gates |  |
| 6 | Draw the Truth Table for Half adder |  |
| 7 | Draw the Truth Table for Half Subtractor |  |
| 8 | How many Full adders are required to add two 16 bit numbers? |  |
| 9 | Draw the block diagram for 4 bit parallel binary adder |  |
| 10 | Convert the binary code 1001 in to its equivalent Gray code |  |
| 11 | Convert the Gray code 1001 in to its equivalent binary code  |  |
| 12 | What is parity bit? What is parity generator and checker circuit? |  |
| 13 | Draw the diagram for 4 bit parallel binary subtractor. |  |
| 14 | Draw the Truth table for EX-OR gate.  |  |
| 15 | Define priority encoder |  |
| 16. | What is multiplexer? |  |
|  |   **PART-B** |  |
| 1 a | Design Half adder and full adder circuits. | 10 |
|  b | What is the design procedure for Combinational circuits ? | 6 |
| 2.a | Design Half subtractor and full subtractor circuits. | 10 |
|  b | Design 2 x 4 Line decoder. | 6 |
| 3 | Design BCD adder | 16 |
| 4 | Design parity generator and Checker circuits. | 16 |
| 5 | Design Binary code to Gray code converter. | 16 |
| 6 | Design Gray code to Binary code converter. | 16 |
| 7 | Design BCD to EX-3 code converter | 16 |
| 8 | Design EX-3 to BCD code converter | 16 |
| 9 | Design 3 X 8 line decoder using basic gates. | 8 |
| 10 | Design 2 bit magnitude Comparator circuit. | 16 |
| 11 | Design BCD to 7 segment display decoder | 16 |
|  | **UNIT-III**  **SEQUENTIAL CIRCUITS** |  |
|  | **PART – A (2 Marks)** |  |
| 1 | What is Sequential circuit? |  |
| 2 | What is Flip-Flop? |  |
| 3 | What are the types of Flip-Flop? |  |
| 4 | Define race around condition in J-K Flip-Flop? |  |
| 5 | What is Edge Triggering? Mention the types of triggering. |  |
| 6 | Write the Characteristic equation for J-K Flip-Flop. |  |
| 7 | Write the Chaacteristic equation for T Flip-Flop |  |
| 8 | Tabulate the excitatio table for J-K Flip-Flop |  |
| 9 | Tabulate the Excitation table for S-R Flip-Flop |  |
| 10 | What is register? Classify it. |  |
| 11 | What are the applications of Shift register? |  |
| 12 | Define Lockout condition in counter. |  |
|  | **PART-B** |  |
| 1 | Explain the operation of R-S Flip-flop | 8 |
| 2 | Explain the Master Slave Flip-Flop | 8 |
| 3 | Construct the D-Flip-Flop by using S-R Flip-Flop | 8 |
| 4 | Construct the T Flip-Flop by using J-K Flip-Flop-Flip | 8 |
| 5 | Design Mod 8 Ripple counter. | 16 |
| 6 | Design Synchronous Decade Ripple counter. | 10 |
| 7 | Design Synchronous 3 bit UP/DOWN counter. | 16 |
| 8 | Design Sync.counter for 4🡪 6 🡪 7 🡪3 🡪 1 🡪4🡪 ……Avoid Lockout condition.Use J-K FF | 16 |
| 9 | Design a Sequence generator to generate the following sequence using D FF  | 16 |
|  | **UNIT IV. SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS** |  |
|  | **PART – A (2 Marks)** |  |
| 1 | Define sequential circuits. |  |
| 2 | List the types of sequential circuits. |  |
| 3 | Draw the diagram for Moore circuit model |  |
| 4 | Draw the diagram for mealy circuit model |  |
| 5 | Define Asynchronous Sequential Circuits. |  |
| 6 | Classify the types of Asynchronous sequential circuits. |  |
| 7 | What are the assumptions made in Fundamental mode ASC? |  |
| 8 | What are the assumptions made in Pulse mode ASC? |  |
| 9 | What is Hazard? |  |
| 10 | What is Static Hazard? |  |
| 11 | What is Dynamic Hazard? |  |
| 12 | Define ASM Chart |  |
|  | **PART-B** |  |
| 1 |  |  |
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|  | An asynchronous sequential circuit is described by the following excitation and output function Y = X1X2 + (X1 + X2)Y Z = Ya).Draw the Logic diagram of the circuit.b).Derive the transition table and output map. | 16 |
|  | An Asynchronous Sequential circuit has two inputs X2 and X1 and one output Z.When X1=0 , the output Z is 0.The first change in X2 that occurs while X1 is 1will cause output Z to be 1.The output Z will remain 1 untilX1 returns to 0. Draw the state diagram,tabulate the Primitive flow table and draw the merger graph. | 16 |
|  | Explain Hazards in combinational circuits. | 8 |
|  | Design the Hazard free circuit for the following Boolean functionF(A,B,C,D) = ∑m(1,3,6,7,13,15) | 8 |
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|  | **UNIT V-MEMORY DEVICES** |  |
|  | **PART – A (2 Marks)** |  |
| 1 | What is RAM |  |
| 2 | List the types of RAM |  |
| 3 | What is ROM? |  |
| 4 | List the types of ROM |  |
| 5 | What is the need of PLDs? |  |
| 6 | What is PLA? |  |
| 7 | What is PAL circuit? |  |
|  | **PART-B** |  |
| 1. | Explain the memory decoding and expansion. | 16 |
| 2. | Explain the Static and dynamic RAM | 16 |
| 3. | Explain all the types of ROM | 8 |
| 4 | Design the PLA circuit for the Boolean functions F1 = ∑m(3,5,7) F2 = ∑m(4,5,7) | 8 |
| 5 | Design the PLA circuit for the Boolean functions A(x,y,z) = ∑m(1,2,4,6) B(x,y,z) = ∑m(0,1,6,7) C(x,y,z)=∑m(2,6) | 8 |
| 6 | Design the PAL circuit for the Boolean functions W(A,B,C,D) = ∑m(0,2,6,7,8,9,12,13) X(A,B,C,D) = ∑m(0,2,6,7,8,9,12,13,14) Y(A,B,C,D)=∑m(2,3,8,9,10,12,13) , Z(A,B,C,D)=∑m(1,3,4,6,9,12,14) | 16 |
| 7 | Design the PAL circuit for the Boolean functions A(x,y,z) = ∑m(1,2,4,6) B(x,y,z) = ∑m(0,1,6,7) C(x,y,z)=∑m(2,6) D(x,y,z)=∑m(1,2,3,5,7) | 16 |
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